900MHz to 1.2GHz Two-Phase Resonant Clock Network with Programmable Driver and Loading

Juang-Ying Chueh, Visvesh Sathe, and Marios C. Papaefthymiou

Advanced Computer Architecture Laboratory, EECS Department
University of Michigan, Ann Arbor, MI 48109
{jchueh, vssathe, marios}@eecs.umich.edu

***Abstract*-A resonant clock network with programmable driver and loading is designed in a 0.13µm CMOS technology. The 2mm×2mm distribution network has on-chip inductors and performs a forced oscillation at the rate of a reference clock programmable in the 900MHz to 1.2GHz range. Clock amplitude and energy efficiency trade-offs at and off resonance are explored with various driver configurations. Energy efficiency per cycle is 1.39 to 1.56 times greater than previous resonant distribution networks.**

I. Introduction

Resonant clock distribution has the potential to reduce clock power and achieve low clock skew and jitter [1, 2, 3]. In this paper, a two-phase resonant clock network with a programmable driver and loading is designed. Unlike [2, 3], where oscillation is free-running and clock frequency is determined by the capacitive and inductive load, this network uses a clock generator that is driven at a reference clock frequency. Moreover, unlike [2, 3], that rely on a current source to control clock amplitude, this design uses the width size and duty cycle of the replenishing switches in the clock generator to adjust clock amplitude. The optimal width size and replenishing pulse duty cycle are explored in this paper. Furthermore, programmable loading allows for different balanced/imbalanced load configurations, enabling the investigation of clock amplitude, power, and skew at resonance and off resonance for operating frequencies in the 900MHz to 1.2GHz range. Included is on-chip circuitry for measuring skew and clock amplitude.

Our results show that the resonant clock system achieves 45% relative power savings over conventional CV^2. The optimal replenishing pulse duty cycle for the clock generator is in the 25-32% range. The optimal clock generator switch size depends on clock amplitude and functionality of loading circuitry. When running off-resonance by 10%, power dissipation increases by 3% and clock amplitude drops by 3%. Imbalanced loading impacts power and amplitude by less than 2%. When shifting from balanced to imbalanced loading, skew increases by 6% of cycle time. Our study is the first investigation of amplitude and energy in resonant clocking at and off-resonance with balanced and imbalanced clock loading.

The remainder of this paper has three sections. Section 2 describes the design of the two-phase resonant clock distribution network. Section 3 presents the chip measurement results. Our contributions are summarized in Section 4.

II. Two-Phase Resonant Clock Network

Fig.1 shows our resonant clock network design. Four 4nH spiral inductors connected in parallel are placed symmetrically around the center of the H-tree clock network. A single central clock generator is used to compensate for power losses and maintain clock amplitude using switches of programmable size *w* that are driven by replenishing pulses of programmable duty cycle *d*. When *Q1* turns on the NMOS switch, the waveform ϕ is pulled down. After half cycle, *Q2* turns on the PMOS switch to pull ϕ up. The complementary phase $\bar{\phi}$ operates similarly with 180 degrees phase delay. The size of the programmable switches *w* ranges from 0µm to 810/405µm for PMOS/NMOS with minimum channel length. The programmable duty cycle *d* of the replenishing pulses ranges from 0% to 44%. Switch sizes and duty cycle can be thus programmed to maintain clock amplitude while minimizing power consumption. The clock network and on-chip test circuitry contribute 31.2pF per phase. The clock network has 16 leaf nodes per phase, each equipped with a clock amplitude detector and programmable switch MOS capacitor C_i (i=1,..., 32) contributing an additional 0pF to 1.3pF (20.8pF per phase in total). These programmable capacitors yield a resonant frequency range from 0.99GHz to 1.27GHz and allow for experimentation with imbalanced loading. A micrograph of the 2mm×2mm clock network is shown in Fig. 2. The chip was designed in a 0.13µm, 8-level (top 2 levels thick) copper CMOS process.

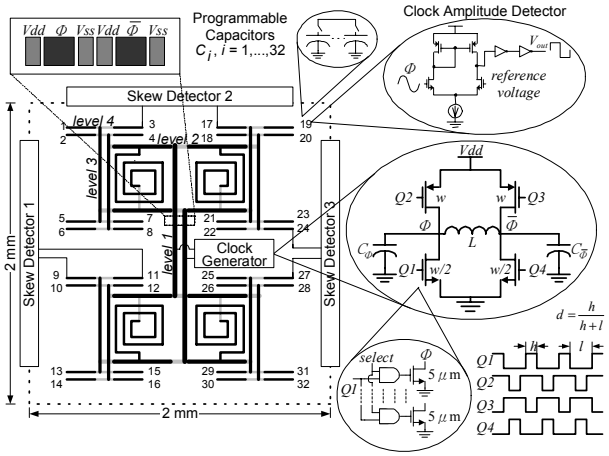

Fig. 1. Two phase resonant clock network.

Table I
Summary of chip performance and comparison with previous work.

	S. C. Chan et al.[2]	This work
Frequency(GHz)	1.6	1
Tracks reference clock frequency	No(free resonance)	Yes(forced oscillation)
Chip size	2mm×2mm	2mm×2mm
Capacitance loading(pF)	13	52
Clock amplitude(V)	Not reported	1.01 to 1.06
Power dissipation(mW)	46.8 (26mA×1.8V)	59 to 87
Energy per cycle(pjoule)	29.3	59 to 87
Energy efficiency relative to [2][a]	1	1.39 to 1.56

[a] Note: Energy efficiency of this chip over [2] is normalized to account for different cycle time, capacitive loading, and clock amplitude. Both networks are assumed to have same resistance. Best-case amplitude of 1.8V is assumed for [2].

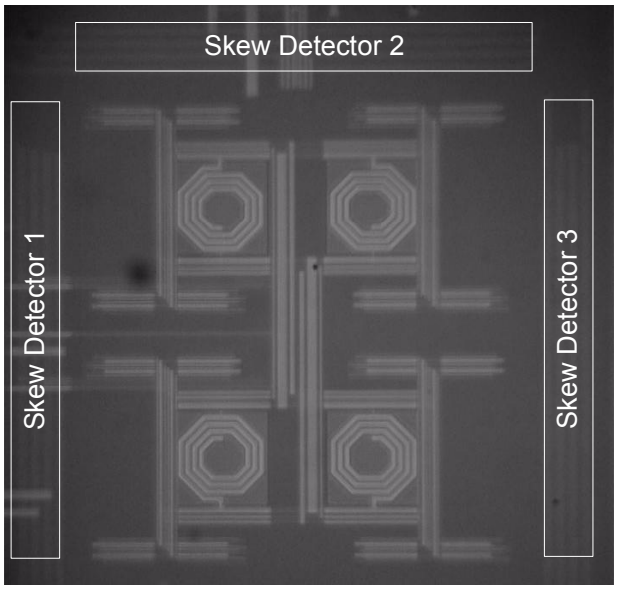

Fig. 2. Chip micrograph.

III. Chip Measurement Results

A. Power dissipation and clock amplitude

Table I summarizes the performance of this chip and compares it with the previous work in [2]. Normalized to account for different cycle time, capacitive loadings, and clock amplitude, the relative energy efficiency of this chip is 1.39 to 1.56 times greater than [2]. Since energy dissipation in resonant networks is given by $(\pi^2/8)(RC/T)CV^2$[4], the normalization factor of the efficiency ratio E_2/E_1 is $(C_1/C_2)^2(T_2/T_1)(V_1/V_2)^2$, where E_1, C_1, T_1, V_1 are the energy, capacitance, cycle time, and clock amplitude in this chip, and E_2, C_2, T_2, V_2 are the corresponding parameters in [2].

Fig. 3 shows measured total power dissipation (including drivers for *Q1* through *Q4*) as a function of operating frequency. All data are obtained with a total capacitance of approximately 52pF (C_i = 1.3pF) per phase, yielding a resonant frequency of 990MHz. For each curve, data points correspond to the pairs (*w, d*) that yield minimum power dissipation at the corresponding operating frequency while maintaining the same average amplitude over all 16 leaf nodes. The curves report average results for 4 test chips. The maximum difference in measured amplitude and power among the 4 chips is less than 6%. Power dissipation is minimized when the system is driven at its resonant frequency. Relative power savings over conventional CV^2 are given as a function of operating frequency. These savings are defined as $1- E_d/CV_a^2$, where E_d is energy dissipation per cycle, C is the sum of capacitive loading of each clock phase, and V_a is the measured *RMS* voltage of the 16 leaf node amplitudes. Maximum relative savings of the resonant system are around 45%. When the system is driven off resonance at 1.1GHz, it dissipates 14% more power, and relative power savings drop by 5% to maintain the same clock amplitude. When the system is driven off resonance at 900MHz, it dissipates 20% more power, and relative power savings drop by 5% to maintain the same clock amplitude.

Fig. 4 shows the shmoo plot of average clock amplitude obtained by varying *w* and *d* when clock network is operating at its resonant frequency (990MHz). All points denoted by the same symbol fall within a 0.06V-wide band of measured clock amplitude. The iso-amplitude bands illustrate the tradeoff between *w* and *d*. Clock amplitude increases with both *w* and *d*. The rectangular region in the middle of the shmoo plot represents the maximum relative power savings configurations.

Relative power savings as a function of *w* and *d* are shown in Fig. 5. The contours on the (*w, d*) plane represent the (*w, d*) pairs for the same savings. The optimal *d* for maximum savings is in the 25%-32% range. At lower *d*, due to lack of conducting time from the power supply, the amplitude is low, hence degrading the savings. At higher *d*, excess power wasted in the clock network decreases savings. For fixed *d*, lower *w* yields better power savings.

From Fig. 4 and 5, it can be inferred that both *w* and *d* play a significant role in controlling clock amplitude and energy efficiency. The optimal *d* for maximum power savings falls in the range of 25-32%. Higher *w* can increase clock amplitude but lower the power savings. Therefore, it is more dissipative and inefficient to maintain higher clock amplitude in resonant clock distribution. In general, larger switches reduce resistance in the clock generator and increase clock amplitude. At the

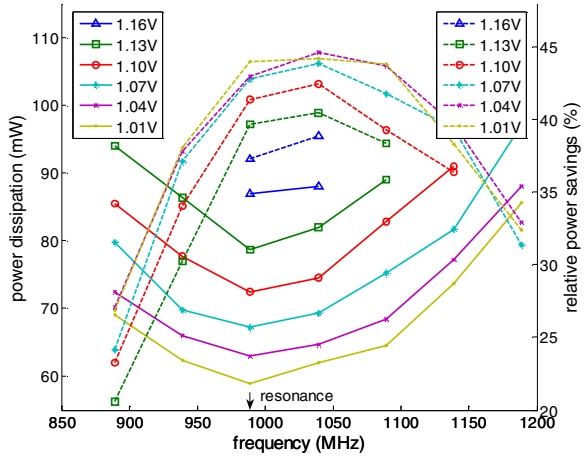

Fig.3. Power dissipation and relative power savings with fixed clock amplitude.

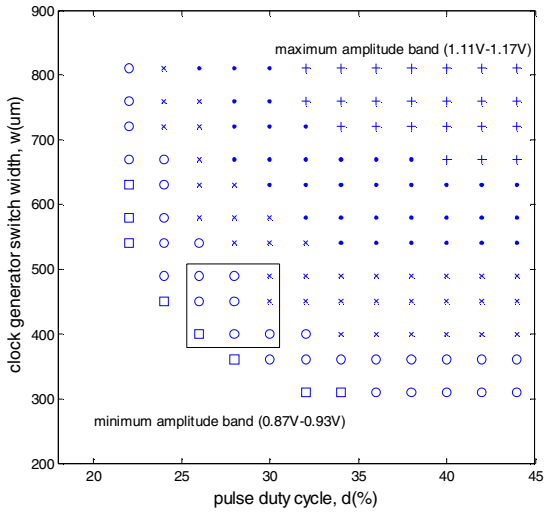

Fig. 4 Shmoo plot of clock amplitude when operating at resonance (990MHz).

same time, they increase dissipation, because dissipation depends quadratically on current. Therefore, the optimal *w* for maximum efficiency might not produce the rail-to-rail clock amplitude, affecting the correct operation of loading circuitry. When determining the optimal *w*, one needs to consider amplitude, energy and correct function of loading circuitry.

Fig. 6 shows measured clock amplitude and power dissipation as functions of frequency for four (*w, d*) configurations at resonance (990MHz). Average results from 4 test chips are reported. When driving frequency is off resonance by 10% at 1.1GHz, power dissipation increases by 3% and clock amplitude drops by 3%. In comparison with Fig. 3, notice how the increase in power is not as high, due to the reduction in the clock amplitude.

Fig. 6 also shows that configurations with larger switch size and replenishing duty cycle 30% can dissipate less power, while maintaining the same amplitude in frequency range of 900MHz to 1.2GHz. The (720µm, 30%) configuration main-

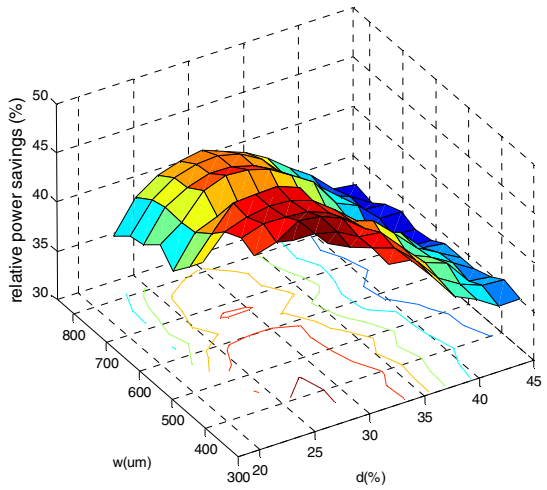

Fig. 5. Relative power savings as a function of *w* and *d* when operating at resonance (990MHz).

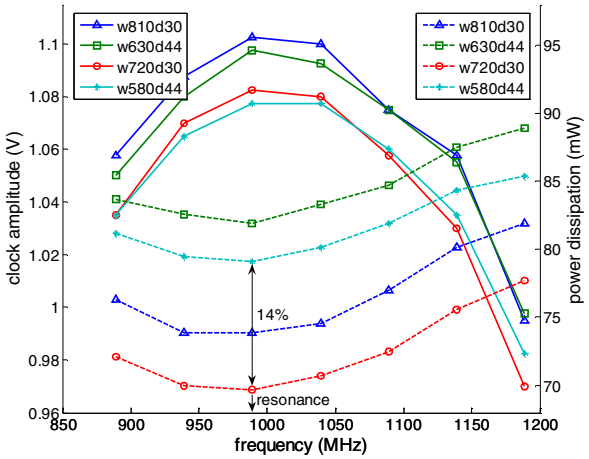

Fig. 6. Clock amplitude and power dissipation for 4 fixed (*w, d*) configurations.

tains slightly higher amplitude than the (580µm, 44%) one, while dissipating 14% less power. The (630µm, 44%) and (810µm, 30%) configurations show similar results, which are consistent with results in Fig. 4 and Fig. 5.

B. Balanced and imbalanced loadings

Measured power dissipation and clock amplitude versus frequency under various clock load distributions are shown in Fig. 7. Data are given for balanced leaf loading (i.e., C_1,..., C_{32} = 0.65pF) and imbalanced leaf loading (i.e., C_1,..., C_{16} = 1.3pF and C_{17},..., C_{32} = 0pF). In both cases, total capacitance per phase is kept at 42pF, yielding a resonant frequency of 1.1GHz. Switch size *w* is set to 810µm, and replenishing duty cycle *d* is set at 32% and 44%, respectively. Our results show that under imbalanced loading, average amplitude and power change by

less than 1.1% and 1.7%, respectively, in comparison with balanced loading.

Skew when shifting from balanced to imbalanced loading is measured from 4 test chips using on chip-skew detectors. Fig. 8 shows measured skew results between leaf nodes 3 and 17. When leaf loading is imbalanced, the additional skew is less than 6% of cycle time.

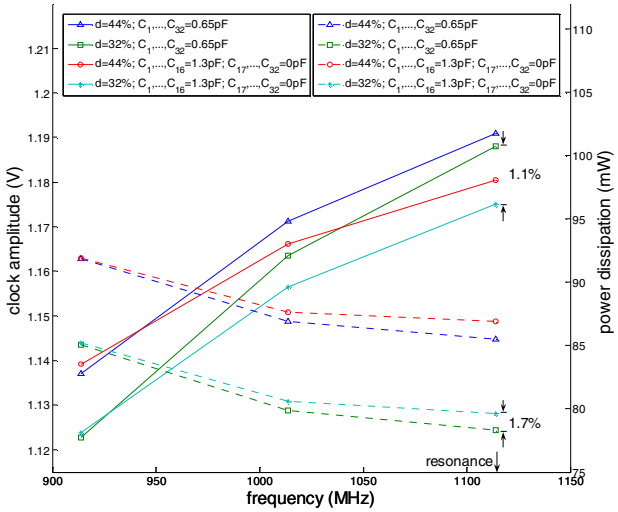

Fig. 7. Clock amplitude and power dissipation under balanced and imbalanced leaf loading.

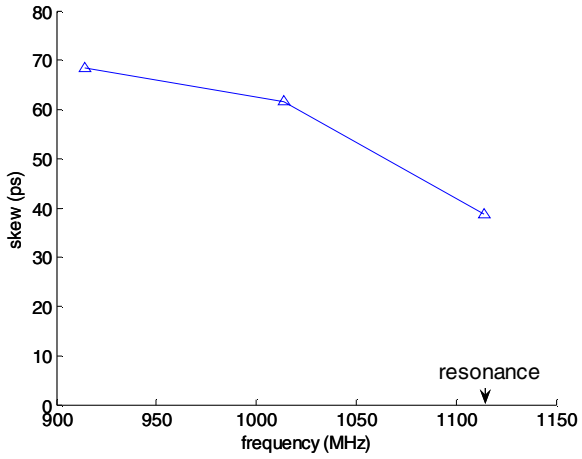

Fig. 8. Skew difference between balanced and imbalanced leaf loading.

IV. Conclusion

This paper presents the design and empirical evaluation of a two-phase resonant clock distribution. Rather than running free, the clock generator tracks a reference clock frequency. The clock generator can control clock amplitude through the programmable size (w) and duty cycle (d) of its replenishing switches. Design guidelines for optimal configuration of (w, d) are investigated. The resonant clock system can achieve 45% relative power savings over conventional CV^2. When running off-resonance by 10%, power dissipation increases by 3% and clock amplitude drops by 3%. Imbalanced loading impacts power and amplitude by less than 2%. When shifting from balanced to imbalanced loading, worst-case skew increases by 6% of cycle time.

References

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