# Fully-Integrated Switched-Capacitor Voltage Regulator with On-Chip Current-Sensing and Workload Optimization in 32nm SOI CMOS

Xiaoyang Mi[1], Debashis Mandal[1], Visvesh Sathe[2], Bertan Bakkologlu[1], and Jae-sun Seo[1]
[1] School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, USA
[2] Department of Electrical Engineering, University of Washington, Seattle, USA

***Abstract*—Efficient, stable, and fast power delivery against fluctuating workloads have become a critical concern for applications from battery-powered devices to high-performance servers. With high density on-chip capacitors, fully-integrated switched-capacitor (SC) voltage converters provide high efficiency down-conversion from a battery or off-chip voltage regulation modules. However, maintaining such efficiency with minimal supply noise across a wide range of fluctuating load currents remains challenging. In this paper, we propose an on-chip current sensing technique to dynamically modulate both switching frequency and switch widths of SC voltage converters, enhancing fast transient response and higher efficiency across a wide range of load currents. In conjunction with SC converters, we employ a low-dropout regulator (LDO) driven by a push-pull operational transconductance amplifier (OTA), whose current is mirrored and sensed with minimal power and efficiency overhead. The sensed load current directly controls the frequency and width of SC converters through a voltage-controlled oscillator (VCO) and a time-to-digital converter, respectively. In 32nm SOI CMOS, the proposed voltage regulator maintains 77-82% efficiency at 0.95V output voltage with less than 20mV steady-state ripple across 10X load current range of 100mA-1A and 33mV droop voltage for a 80mA/ns load transition, while providing a projected current density of 6W/mm$^2$.**

***Keywords—on-chip current sensing; switched-capacitor voltage converter; voltage-controlled oscillator; low-dropout regulator.***

## I. INTRODUCTION

In recent years, on-chip integrated voltage regulators have received much interest for providing a fully integrated solution that offers high-voltage delivery and fast response to fluctuating workloads. Linear regulators or low-dropout (LDO) regulators are compact and fast but offer poor efficiency when the difference between input and output voltage is considerable [1-2]. Compared to buck converters with high-quality off-chip or package-integrated inductors [3-4] providing high efficiency across a wide output voltage range, on-chip buck converters [5-6] still suffer low efficiency and low current density due to low-quality and bulky inductors. Fully-integrated switched-capacitor converters [7-15] offer high efficiencies at integer step-down conversion ratios, and high current density could be achieved using high-density on-chip capacitors [10-13]. Still, maintaining high efficiency of switched-capacitor converters amidst significant workload fluctuations is a challenging task since multiple design parameters such as switching frequency and switch widths need to be dynamically adapted in a fast manner to minimize loss corresponding to load current change.

Literature on the voltage regulation of switched-capacitor converters has primarily focused on output voltage comparison against reference voltage [7-15]. The approaches that attempted to optimize both switching frequency and width (or phase partition) either required several reference voltages to make a two-dimensional decision [8, 14], or was handicapped by the amount of tuning capability per clock period [9].

We postulate that the optimal way to modulate the frequency and width of SC converters simultaneously is to instead, sense the on-chip load current and directly apply the information into the modulation, such that the switched-capacitor voltage converters are promptly driven into the most efficient state with respect to the workload. On-chip current sensing has been employed in a number of previous buck converter designs for the purpose of current-mode feedback control [16-18]. However, load current sensing has not been largely adopted for SC converters, since they are mainly based on voltage-mode charge and discharge operations.

In this paper, we propose to integrate on-chip current sensing circuitry in the closed-loop regulation of a 17-phase 2:1 SC converter, whose target input voltage is 2.1V and output voltage is 1V. Noting that SC or buck converters are accompanied by linear regulators for fine-grain regulation and control [9, 19], our SC converter is followed by a low-dropout (LDO) regulator with ~50mV dropout, which is driven by a push-pull operational trans-conductance amplifier (OTA). 1/1000 scale of the LDO current is sensed, minimizing the sensing area and power overhead. The sensed current directly drives the current-starved voltage-controlled oscillators (VCO) for continuous switching frequency modulation, and a time-to-digital converter (TDC) compares the VCO phase delay with a reference delay to modulate the discrete switch width. Across 100mA-1A load currents, the proposed design achieved 20mV steady-state ripple and nearly constant efficiency of 80%, and the voltage droop was kept under 33mV for an 80mA/ns load transient.

We focus on a 2:1 SC voltage converter design throughout this paper, but the proposed current-sensing-based workload optimization technique can be applied to other integer voltage conversion ratios [7, 8, 13]. On the other hand, recently proposed fine-grain SC voltage converters employed only 2:1 converters in successive approximation [14] or in a recursive manner [15], which makes the design optimization of 2:1 SC converter design optimization particularly relevant.

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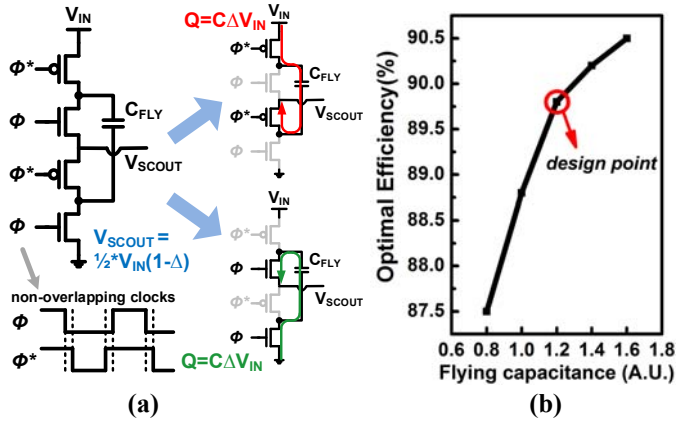


**Figure 1. (a) Basic operation of the 2:1 SC converter. (b) Optimum efficiency of SC converter with different flying capacitance values ($V_{IN}$=2.1V, $V_{OUT}$=1V, $I_{OUT}$=59mA).**

## II. Single-Phase Switched-Capacitor Voltage Converter Optimization

In this section, we investigate optimization of a single-phase 2:1 SC voltage converter. The results will be applied to the multi-phase interleaved SC converter design in Section III.

### A. 2:1 Switched-Capacitor Converter Operation

A 2:1 SC down-converter operates with non-overlapping clock signals applied at different switch devices [7, 11, 12], as illustrated in Figure 1(a). In one state, the top and bottom plate of the flying capacitor is connected to the input voltage ($V_{IN}$) and the output voltage ($V_{OUT}$), respectively. In the other state, the top and bottom plate of the flying capacitor is connected to the output voltage ($V_{OUT}$) and ground, respectively. Continuously switching back and forth between the two states, the input voltage is effectively divided by half, providing a 2:1 down conversion. To maximize the conversion efficiency, the power loss due to switch devices, drivers, bottom-plate capacitance, and inherent ripple should be balanced and minimized based on load current ($I_{LOAD}$).

Our target load current is 1A, which would be similar to those of mobile application processors (AP). Assuming that leakage power could consume at least 10% of the total AP power, the SC converter should adapt to 10X range of current from 0.1A to 1A. With target load current at given $V_{IN}$ and $V_{OUT}$ voltages, the design parameters of the SC converter include switch width, switching frequency, and flying capacitance, which affect the overall efficiency and current density.

### B. Optimal Efficiency and Power Density Trade-off

Assuming that 17 SC converter phases will be interleaved to reduce inherent ripple (detailed description in Section III), the single-phase SC converter should produce output current of 58.8mA (1A/17). With ideal voltage sources of 2.1V and 1V connected at $V_{IN}$ and $V_{OUT}$, respectively, we performed a coarse three-dimensional sweep of switch width, switching frequency, and the flying capacitance ($C_{FLY}$). For five $C_{FLY}$ values, both the switch width and frequency are swept in simulations using 32nm technology, where the flying capacitors are implemented with the deep trench capacitors. Figure 1(b) shows the optimal efficiency for each $C_{FLY}$, which could be viewed as the efficiency and power density trade-off, since $C_{FLY}$ occupies a dominant part of SC converter area. The knee point in the curve in Figure 1(b) is chosen as our design point for the single-phase $C_{FLY}$. Conservatively, if 20% of the total regulator area is devoted to circuits other than $C_{FLY}$, 6W/mm$^2$ power density could be achieved at this design point.

### C. Frequency and Width Optimization with Load Current

The authors in [7] showed that both the optimal switch width and switching frequency is proportional to $(I_{LOAD})^{2/3}$. More recently, it has been shown that in the case of output-resistance constrained 2:1 SC converters, switch-width and switching frequency should both scale linearly with target output resistance [21]. With the $C_{FLY}$ from Section II.B, we explored the two-dimensional design space of frequency and switch widths of the 2:1 SC converter in 32nm technology for load currents from 100mA to 1A (Figure 2), to quantify the importance of such co-optimization. As in Section II.B, $V_{IN}$ and $V_{OUT}$ are connected to voltage sources, and power losses for control or regulation were not considered.

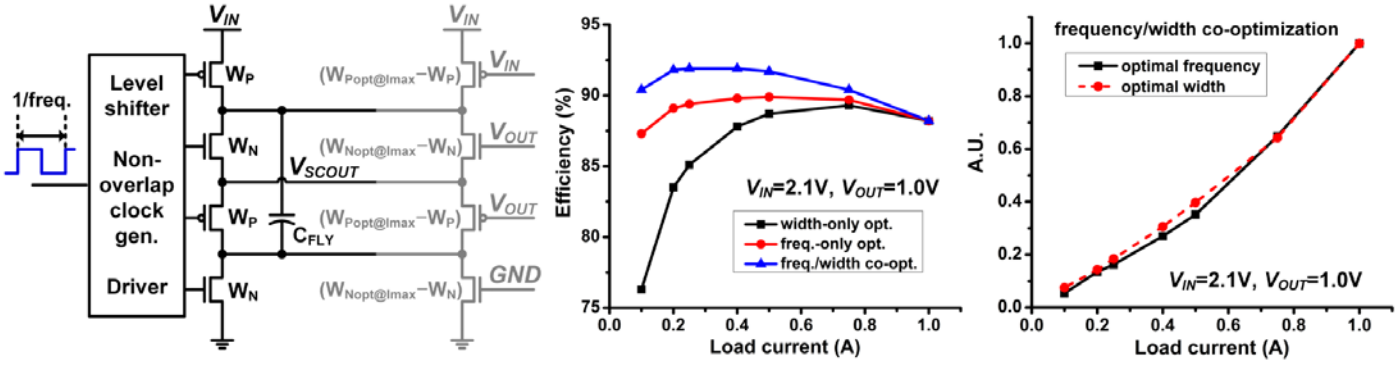


**Figure 2. (a) 2:1 switched-capacitor converter schematic with on-/off-branch is shown. (b) Ideal efficiency comparisons with optimal frequency and/or width modulation for 100mA-1A load currents are shown. (c) Relative value of optimal frequency and width for 100mA-1A load currents are shown.**

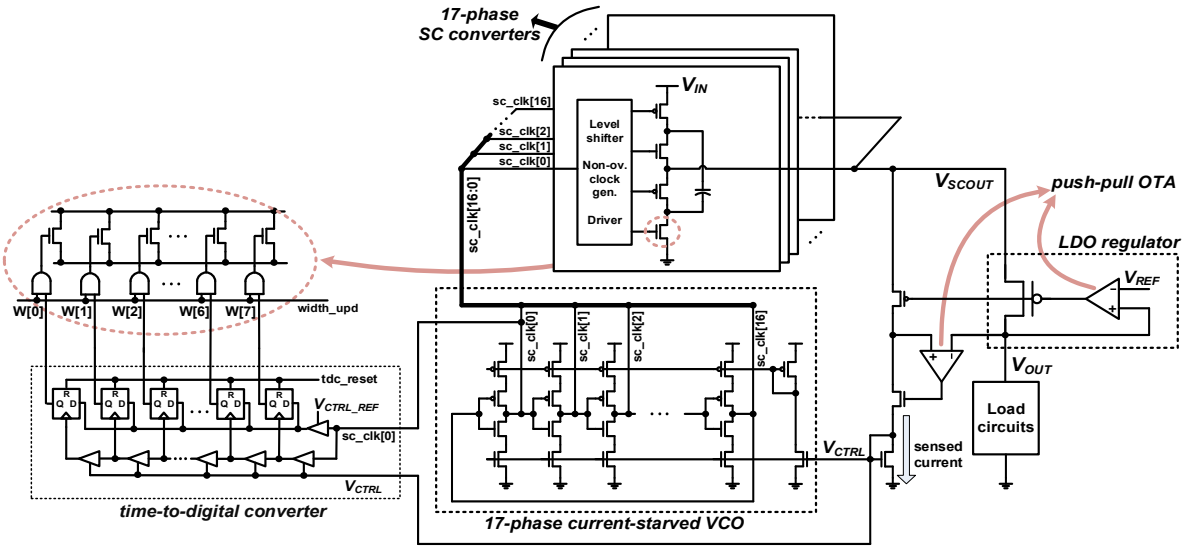


**Figure 3. Proposed switched-capacitor voltage regulator with on-chip current sensing.**

We first found the optimal width and frequency for the maximum current of 1A, and the resulting width (Wopt@Imax) was used as the total width of the on-branch and off-branch of the switches (Figure 2(a)), such that the effect of parasitic capacitance is captured in width modulation. Through stacking, since no transistor in the converter or driver sees voltage larger then ($V_{IN}$-$V_{OUT}$), only thin-oxide devices are used without reliability concerns.

The two design parameters were then swept to find out the optimal frequency and width that led to the best efficiency at different load current values, and the results are shown in Figure 2(b). Figure 2(c) shows the relative value of both switching frequency and switch width of SC converters for the 10X range of load currents, where 10-20X adaptation in frequency and width is shown to be necessary to optimize the efficiency across the target load range.

## III. Fully-Integrated Switched-Capacitor Voltage Regulator with On-Chip Current Sensing

Figure 3 shows the proposed fully-integrated SC voltage regulator with on-chip current sensing. Design components that constitute the overall voltage regulator will be described in this section.

### A. 17-Phase SC Converter

Starting from the single-phase SC converter optimized in Section II, multiple-phase interleaving was adopted to reduce the inherent output voltage ripple and enhance response time [7, 10, 13]. The clock signals of multiple converter phases were driven by a 17-phase voltage-controlled oscillator (VCO), whose frequency is controlled by current-starved footers and headers. The number of phases was chosen as 17, since it showed a good trade-off between ripple reduction and converter design overhead. The number of configurable switch widths was chosen to be eight (with half-LSB switch always on), to balance width configurability and parasitics of the switch devices. Using eight discrete widths, there was <0.3% efficiency degradation from the ideal achievable efficiency with continuous widths in Figure 2(b).

### B. On-Chip Current Sensing and LDO Regulator

To sense the load current, we chose to use a LDO regulator in conjunction with step-down SC converters [9, 19], which also provide benefits such as fine-grain voltage output and ripple minimization. The current sensor is realized by a parallel PMOS transistor that is matched to the power PMOS transistor in the LDO regulator with a 1:1000 size ratio [18].

As shown in Figure 3, the error amplifier in the LDO regulator controls the strength of the power transistor such that the output voltage ($V_{OUT}$) tracks the desired reference voltage ($V_{REF}$). To accurately sense the load current with a linear ratio, another operational amplifier is employed to keep the drain voltages of the power and sensing PMOS transistors very close to each other. For the frequency modulation, the sensed load current directly controls the delay of the VCO, which modulates the frequency of the 17-phase switched-capacitor converters. For the width modulation, the sensed current goes through a time-to-digital converter that provides an 8-bit thermometer code that controls the switch widths of all 17 phases.

### C. Push-pull OTA with Channel-Resistance-Insensitive Small-Gain Stages

The error amplifiers in the proposed design largely affects the performance of the voltage regulator, including DC error, voltage droop, and steady-state ripple of the regulator output. The short-channel effects in the 32nm process must be considered carefully in the operational amplifier design to ensure high specifications such as gain, bandwidth, and phase margin. To that end, we present a differential operational transconductance amplifier (OTA) with a push-pull output stage. Differential implementation has been adopted in this design instead of conventional single-ended cascaded gain-boosting stages.

Figure 4 shows the proposed design of a push-pull OTA that provides gain boosting, wide output swing, as well as a push-pull output stage for symmetric ripple cancellation. In the differential input stage, negative-$g_m$ method is applied for gain-boosting by increasing the output resistance. The intermediate cascaded stages are channel-resistance-

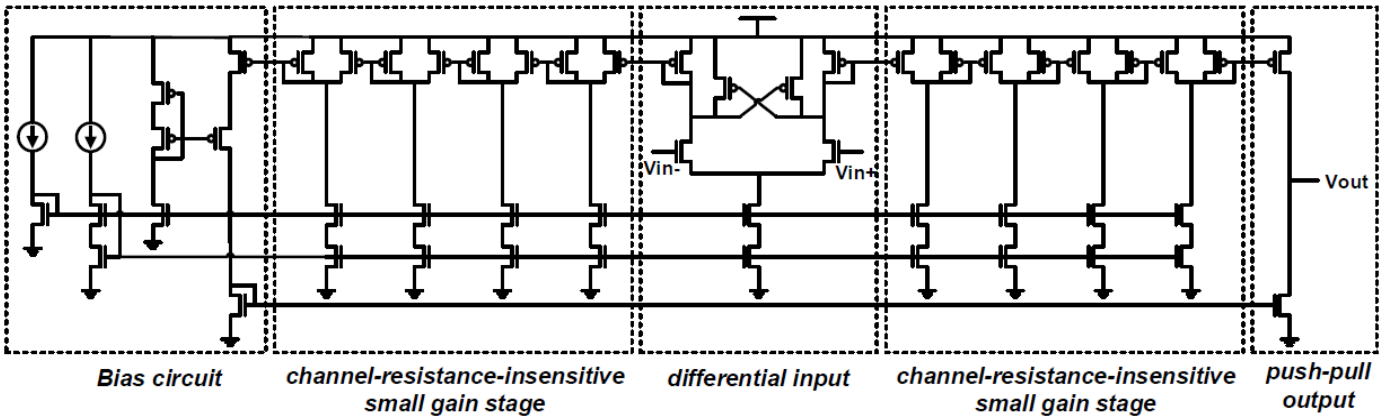


**Figure 4. Push-pull OTA with channel-resistance-insensitive small-gain stages.**

insensitive, which offers small gain and less-dominant poles and zeros to keep sufficient bandwidth while enhancing the DC gain [20]. Meanwhile cascode tail-biasing in these small-gain stages alleviates the, current mismatch issue in the SOI process.

Due to different emphasis on the two error amplifiers, trade-offs are made to properly design the two OTAs separately. First, the LDO error amplifier requires high DC gain, high bandwidth, and moderate phase margin to ensure output voltage accuracy and fast response to load transients. On the other hand, the error amplifier employed for current sensing requires higher phase margin to maintain the current sensing loop with minimal noise and ripple, especially on the feedback control voltage from the diode-connected NMOS transistor. To that end, the error amplifier for the LDO contains four cascaded small-gain stages while the error amplifier for current sensing was designed to have three small-gain stages, where the degraded loop gain due to less cascading still offers a current sensing accuracy of 97.3% to 100% across the load range, as shown in the experimental results. Bias currents of the push-pull output stage of the error amplifiers are set properly to satisfy the stability and dynamic performance requirements of both the LDO and the current sensing feedback loops.

### *D. Voltage-Controlled Oscillator*

As shown in Figure 3, the sensed current is mirrored and directly drives the footer and header of the current-starved voltage-controller oscillator. Through this tight integration, the sensed current promptly modulates the SC converter frequency in a continuous fashion. The footers and header sizes determine the amount of starved current for charging and discharging the output capacitance of each inverting stage, and the inverters Push-pull OTA Performance that reside between the header and footer are sized accordingly to obtain the targeted frequency range with the feedback control voltage.

### *E. Time-to-Digital Converter*

To perform the discrete switch width modulation, the time-to-digital converter shown in Figure 3 converts the sensed current into digital signals that turn the switches on or off. The chain of the eight delay stages are controlled by the same feedback voltage used in frequency modulation. Each delay stage is equivalent to a single VCO phase, varying with the load current through the feedback control voltage. This is compared with a reference delay, and counts how many flip-flops the delay driven by current sensing will go through in a given time. Instead of converting linear delay into linear digital values, this design converts linear current, to which the corresponding delay is inversely proportional, into linear digital values.

## IV. Experimental Results

The proposed integrated SC voltage regulator with on-chip current sensing was designed and simulated in 32nm SOI CMOS with deep trench capacitors. We also implemented a baseline switched-capacitor voltage regulation scheme that performs pulse frequency modulation [10, 13] for comparison. Regulator efficiency, voltage droop against load transients, and steady-state ripple across 10X range of load currents will be reported in this section.

### *A. Push-pull OTA Performance*

Figure 5 shows the stability simulation results of the proposed push-pull OTA connected to the LDO regulator for maximum and minimum load currents. The LDO error amplifier design achieves a DC gain of 57.2dB with 393.2MHz bandwidth, and 62 degree of phase margin at 1A load current, while for 100mA load current, 60.2dB DC gain with 534.4MHz bandwidth, and 46 degree of phase margin are achieved. In the current sensing OTA, for 1A load current, the achieved bandwidth and phase margin are 307.4MHz and 78.5 degree, with a DC gain of 35.7dB, and for 100mA load current, these values are 579.0MHz and 52.8 degree, with a

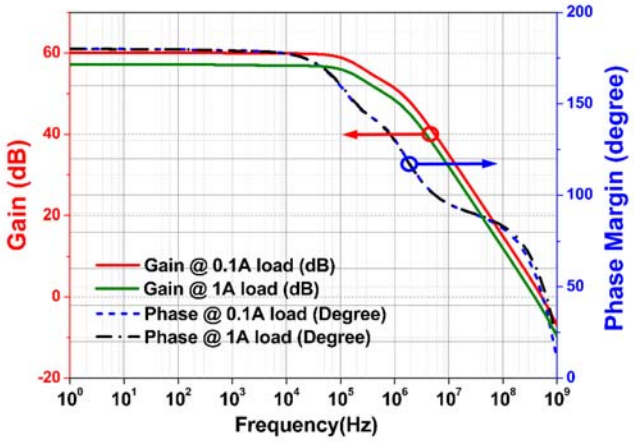


**Figure 5. Loop stability simulation of the LDO push-pull OTA at 0.1A and 1A load currents.**

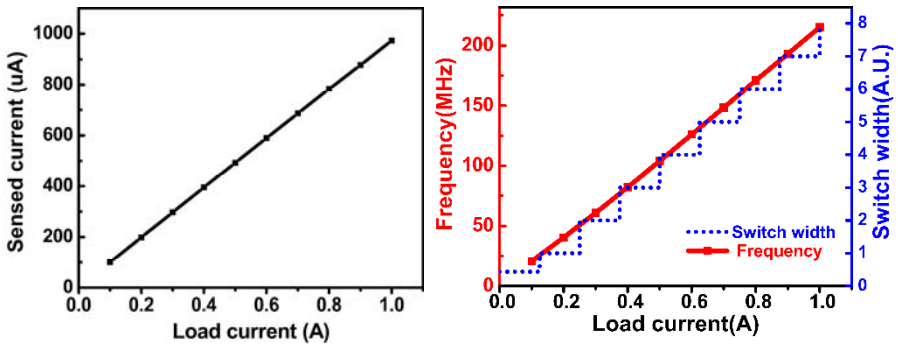


**Figure 6. (a) The accuracy of load current sensing. (b) Continuous frequency modulation and discrete width modulation based on sensed current.**

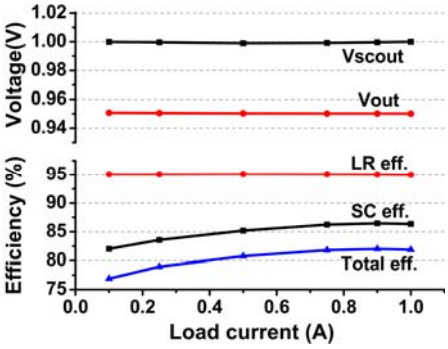


**Figure 7. Output voltage and efficiency simulation results.**

DC gain of 43.1dB. The power consumptions of the error amplifiers for the LDO and current sensing are 751µW and 622µW, respectively.

*B. Regulator Efficiency Across a Wide Load Range*

Figure 6(a) shows the accuracy of the sensed current compared to the actual load current, which depicts a near-linear relationship. Based on the sensed current, the converter switching frequency and switch widths are modulated simultaneously and independently, and the results are shown in Figure 6(b). The current sensing and frequency modulation results show good linearity and exhibit high similarity with ideal results from Figure 2(c). In Figure 7, the output voltages of the SC converter and the LDO regulator, as well as the efficiencies of the SC converter, LDO regulator, and the entire regulator are shown. Overall, a nearly constant efficiency of80% is demonstrated across load currents from 100mA to 1A. Targeting 0.95V, the average output voltage DC error of the regulator is kept under 1% across 10X load range.

*C. Load Transient and Steady-state Regulation*

An abrupt load transient was simulated by transitioning the load current from 100mA to 900mA in 10ns (80mA/ns), and the simulation results are shown in Figure 8. For the width modulation, we assumed that an architectural preset signal could be provided to the regulator [5] earlier than the worst-case load transient, such that the switch widths are pre-configured to maximum width. The error amplifier output promptly tracks the load current change and the SC converter switching frequency is modulated instantaneously without a high-speed clock. As a result, the proposed SC voltage regulator achieves a fast and stable load transition with 33mV of output voltage droop. Without the architectural preset signal, the worst-case droop was 85mV for 80mA/ns load transient, and was 28mV for 16mA/ns load transient. After the load transient occurs, the error amplifiers and the overall regulator promptly stabilize within 15ns.

Figure 9 shows the steady-state voltage waveforms from 100mA to 1A of load current in the steps of 100mA. Aided by the proper designs of the LDO and sensing push-pull OTAs, the steady-state output ripple, the feedback control voltage of the sensing circuitry, and the VCO switching frequency are regulated well with minimal noise and ripple. Across the 10X range of load currents, the worst-case output voltage ($V_{OUT}$) ripple is 20mV at 0.1A load.

*D. Comparison with baseline SC regulator using PFM*

A number of prior works in SC voltage regulation uses pulse frequency modulation (PFM) with a multi-GHz high-speed clocked comparator [8, 9, 10, 13], as illustrated in Figure 10(a). A comparison is made every clock cycle between $V_{OUT}$ and $V_{REF}$, which either enables advancing the next SC converter phase or stall the phase operation until $V_{OUT}$ becomes smaller than $V_{REF}$.

We employed an ideal 3.8GHz clocked comparator, which is equivalent to 17 times the maximum VCO frequency of the proposed design. Without the current sensing circuitry, the

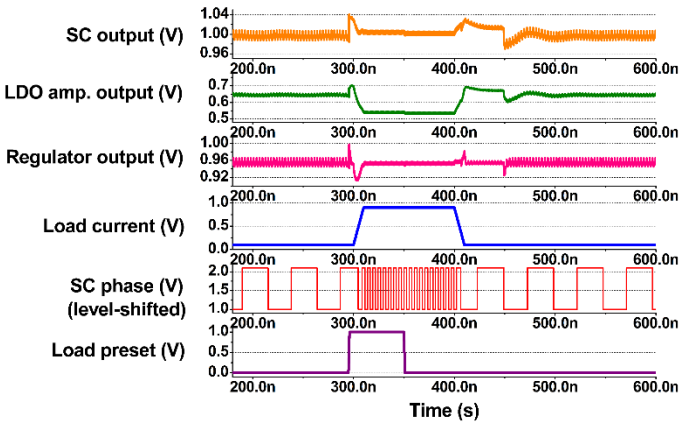


**Figure 8. Transient response of the proposed SC voltage regulator against an 80mA/ns load transition (100mA to 900mA change in 10ns) is shown.**

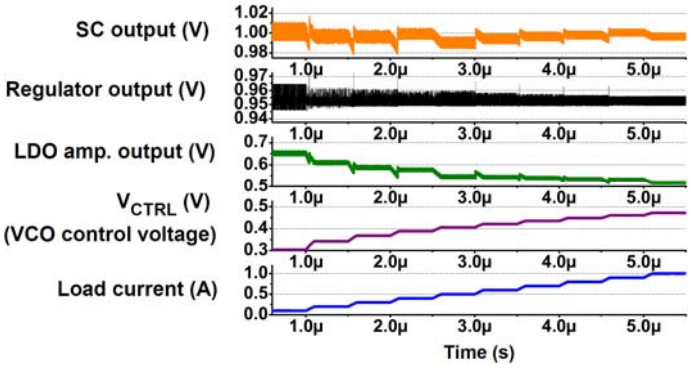


**Figure 9. Steady-state simulation of the proposed SC voltage regulator. While load current is increased at a step size of 100mA from 100mA to 1A, output and intermediate voltage waveforms are shown.**

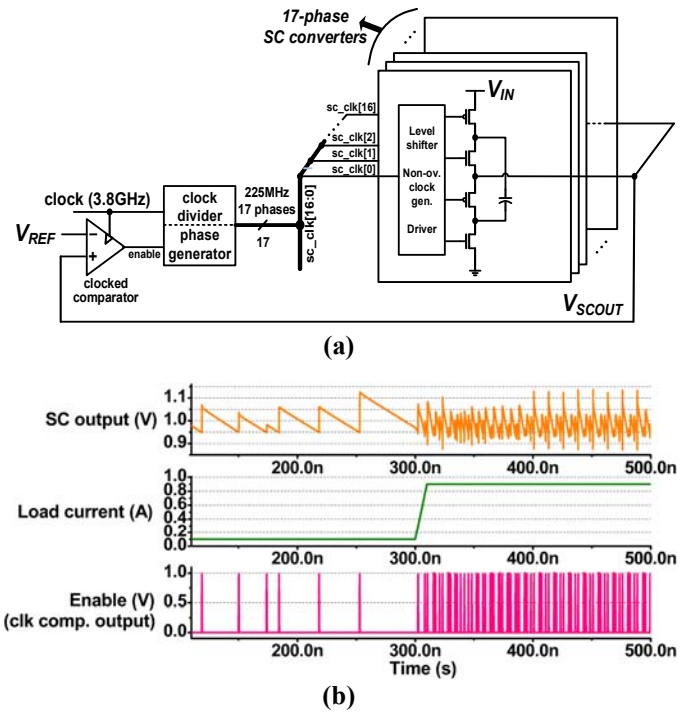


**Figure 10. (a) Baseline SC regulator implementation using pulse frequency modulation (PFM). (b) Load-transient simulation results of the baseline PFM scheme.**

clocked comparison against $V_{REF}$ of 0.95V modulates only the switching frequency, while the switch widths are kept at maximum width. Targeting the same $V_{IN}$ and $V_{OUT}$ voltages with the proposed scheme, identical load transients were applied to the baseline PFM regulation scheme, and the simulation results are shown in Figure 10(b). The worst-case droop for 80mA/ns load transient is 75mV for the SC converter output, while the worst-case ripple is 175mV at 0.1A load. Overall, the proposed scheme improved output voltage droop by 2.2X and the output ripple by 8.7X. Moreover, as expected from Figure 2(b), the efficiency of the proposed scheme was higher than the baseline PFM scheme across the 10X load current range by up to 3%.

## V. CONCLUSION

In this paper, we proposed a fully-integrated switched-capacitor voltage regulator with deep trench capacitors that employs on-chip current sensing to modulate switching frequency and switch widths simultaneously. Experimental results from 32nm simulation achieved 77-82% efficiency across a 10X range of load currents with 6W/mm$^2$. Moreover, a fast and stable 80mA/ns load transition with 33mV droop voltage, and less than 20mV steady-state ripple across the 10X load range is obtained. Future work will include efficiency improvement through lossless current sensing-based converter modulation, and applying the proposed technique to more conversion ratios in reconfigurable SC converters.

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