A Deterministic-Dither-Based, All-digital System for On-chip Power Supply Noise Measurement

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ABSTRACT

Supply-noise measurement techniques are becoming increasingly critical in modern digital design, driven by the trend toward smaller, lower-voltage domains. All-digital measurement modules capable of meeting bandwidth and resolution requirements would enable spatially fine supply voltage measurements across Systems-on-Chip. Existing implementations either use analog techniques, limiting their applicability, or do not meet the increasingly challenging requirements of supply noise measurement. In this paper we discuss a bandwidth-resolution-reconfigurable all-digital system that relies on a dithering technique to achieve a resolution of 2.05 mV at a bandwidth of 6.94 GHz in an industrial 65 nm CMOS process.

1. INTRODUCTION

A substantial amount of supply-voltage margin applied to modern digital designs is attributable to the inductive ($L^{di}/_{dt}$) and resistive (IR) power supply droop observed on-chip. As supply voltages continue to scale driven by the need for energy efficiency, the ability to detect and measure supply noise in post-silicon testing for supply noise mitigation is becoming an increasingly important aspect of efficient, high-performance digital design, particularly in modern SoC designs.

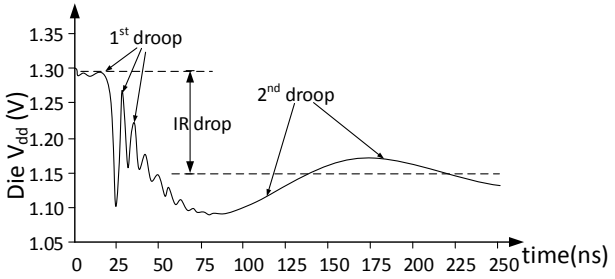

Figure 1: Typical $L^{di}/_{dt}$ and IR supply noise in digital integrated circuits

Figure 1 illustrates the on-die supply voltage resulting from an instantaneous load current increase in a regulated voltage domain of a microprocessor. Inductive supply noise in the form of 1^{st} and 2^{nd} droop occuring at relatively lower frequencies has traditionally been dominant in digital integrated circuits. However, recent integration trends, including three-dimensional integration through chip-stacking [6] and the deployment of multiple voltage domains using integrated low drop out regulators (LDOs) [11], have resulted in increased amplitude and frequency content of supply noise. Increased per-domain package supply impedance, reduced power routing, and decap resources cause faster $L^{di}/_{dt}$ ringing and increased IR drop.

Integrated circuits are needed to adapt to and mitigate supply noise at design time [4, 8]. Detailed post-silicon testing plays a key role in validating and optimizing these techniques and in providing sufficient learning to drive future changes. Modern digital systems require diagnostic supply noise measurement circuits which offer a small footprint, high voltage precision, and meet increasingly demanding bandwidth requirements. Implementing all-digital measurement circuits offers key additional advantages, including easy inclusion within multiple SoC sub-modules and enhanced portability from one process generation to the next.

One common digitally-compatible technique for measuring supply voltage involves using a ring oscillator (RO) as a time-to-digital converter (TDC). The temporal resolution offered by the approach for a given bandwidth is inadequate for current and future power supply noise measurement needs. A number of other supply measurement circuits have been proposed in the literature [1, 5, 9, 10]. Analog implementations tend to have large footprints, do not scale well and are not easily integrated into the design flow. Existing all-digital implementations have also been proposed, but as discussed in Section 2, these techniques place significant practical limitations on the system-under-test such as excessive test time, limited test-pattern length, or an inadequate bandwidth-resolution ratio.

In this paper we propose an all-digital power supply noise measurement circuit that has a small footprint and is capable of high-bandwidth high-resolution measurements with acceptable test time. The proposed technique achieves an elastic, user-tunable bandwidth-resolution ratio of 3.4 GHz/mV. The measurement performance in the circuit is enabled by two key techniques. The first involves periodically sampling the supply noise waveform, similar to [1, 5, 10]. The waveform is iteratively sampled with a small timing window to accumulate large counts. Second, we propose a novel approach involving the application of *deterministic* dither to the sampling window width to suppress quantization error over aggregate measurements, enhancing the bandwidth-resolution ratio beyond what is possible with undithered measurements.

This paper is organized as follows: Section 2 discusses the current state-of-the-art in all-digital supply noise measurement. Section 3 introduces the proposed supply noise measurement system

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and examines its bandwidth-resolution performance. Post-layout simulation results for the proposed measurement circuit are presented in Section 4.

2. RELATED WORK

The use of a ring oscillator (RO) to measure supply voltage is a is one of the oldest known approaches. The RO is started at a defined time and the number of oscillator transitions occurring in a sampling window are counted. Allowing τ denote the voltage-dependent delay of an inverter stage, a sampling duration of T_{samp}, the voltage resolution δ_V can be shown to be $\delta_V = {\tau^2}/{\left(T_{samp}\frac{\partial\tau}{\partial V_{dd}}\right)}$. Improving voltage resolution (lower δ_V) requires lower τ (process limited) or increasing T_{samp} (bandwidth-limiting). Denoting f_{BW} as the 3 dB measurement bandwidth of the technique (approximated as a square-pulse sample), the bandwidth-resolution ratio of the approach is derived to be $\frac{f_{BW}}{\delta_V} = \frac{0.44}{\tau^2}\frac{\partial\tau}{\partial V_{dd}}$. This is insufficient for most SoC applications. In a technology with an inverter delay of 40 ps at 1 V, achieving 6.5 mV resolution limits the bandwidth to approximately 75MHz, inadequate even for 1^{st} droop.

Several enhanced techniques have also been proposed, which rely on the idea of iterative sampling, illustrated in Figure 2. Sampling a narrow time-interval iteratively, and accumulating phase and quantization information enables bandwidth-resolution ratios beyond that possible with traditional RO voltage sensing [1, 9]. In [1], a uniform, randomly distributed initial phase within the RO is assumed to produce transition counts within a sampling window over multiple tests. This technique achieves an excellent bandwidth-resolution ratio, but the statistical measurement approach requires an extremely large number of iterations, making the test time impractical for supply noise measurement in several SoC and multi-core applications. For example, achieving a 3.25mV voltage resolution requires 1.6×10^5 samples. Analyzing a 200ns section of a 3ms code-trace to capture supply noise in a multi-core system [7] (assuming no I/O is required between successive tests) will require an impractical 666 hours of test time with this technique.

More recently, gated ring oscillators have been proposed to deterministically achieve bandwidth-resolution improvement over traditional RO voltage sensing [9]. Quantization error from an individual sample is accumulated between successive iterations in floating node voltages of the gated RO. However, as discussed in [9], charge leakage in scaled CMOS limits the duration of the test to approximately 100ns, making it unsuitable for most practical test vectors. A latched ring oscillator similar to Figure 2 is proposed to address the test duration limitation. However, this approach is identical to a traditional RO based measurement with stage-level counter resolution. A simulated voltage resolution of 40mV with a 1.6GHz bandwidth for the latched RO is reported in [9]. This is insufficient resolution for most measurement applications.

There are a number of analog-based measurement systems proposed [5, 10]. However, such analog techniques are not readily portable, and either area intensive or need a high frequency analog I/O, making them unsuitable for spatially-fine supply voltage measurements required by modern SOCs.

3. PROPOSED APPROACH

This section outlines the proposed all-digital power supply measurement technique. It relies on periodically sampling the supply noise with a deterministically-dithered pulse to achieve substantially finer resolution than a unit RO stage delay.

In the proposed approach, a latched RO topology similar to the one shown in Figure 2 was chosen to support an arbitrarily long test duration. For simplicity, Figure 2 illustrates the principle of operation on a single inverter. Signal in transitions, causing out to transition after $\tau(V)$. A sampling pulse asserted at the same time instant has its width deterministically-dithered from T_{min} to T_{max} over successive iterations. Only iterations where the sampling width exceeds the inverter delay will register a transition at out. Repeated measurements over a range of *uniformly* distributed pulse widths will result in an aggregated edge-count that is proportional to the ratio between the *"edge"* region in the figure and the dither range T_d. Lower voltages with higher delays ($V1 > V2$) result in narrower *"edge"* regions and lower counts. The supply noise sample is periodically generated. The applied deterministic dither exceeds the inverter delay ($T_d > \tau(V)$) and occurs over fine, discrete time intervals. To the first order, the voltage resolution achieved by this approach is determined not by the size of the RO stage delay but by the much finer dither step size.

3.1 Timing Generation

Figure 3 illustrates the system level architecture of the power supply measurement circuit. The timing generation block produces a sampling pulse, φ, that gates a ring oscillator. The width of this pulse is deterministically dithered with sub-picosecond resolution. The timing block also controls the arrival time of the sampling pulse relative to the system clock to perform a supply measurement "sweep" over the test duration.

The timing state-machine relies on its own ring oscillator for both coarse and fine delay, enabling a time offset in the sampling pulse relative to the system clock. The appropriately delayed transition is selected by a multiplexer (MUX) to generate a one-shot $edge\_en$ pulse. Interpolators, controlled by the state-machine, are used for generating fine-delay offsets (sub-gate delay), and for generating the deterministic dither. The fine-delay interpolator operates over a range equal to the unit delay of the timing-generator RO. Two additional interpolators provide the required deterministic dither to incrementally modulate the sampling pulse width over the dither range across successive sampling iterations. The resulting dithered pulse samples the latched RO. The pulse width is first gradually increased by delaying the falling edge of the pulse over multiple iterations and subsequently reduced by delaying the rising edge of the sampling pulse across multiple iterations. Transitions across all iterations needed to implement the uniform deterministic dither and the final state and count of the latched RO is recorded.

The phase interpolator design, shown in Figure 3, is identical across all three instantiations. The interpolator decode logic sets *clkD<63:0>* bits thermometrically to $count$, modulating nMOS current drive and causing a linear increase in edge transition delay. A fully-static interpolator design is used to generate 64 different delay values. The control logic is capable of implementing dynamic-element-matching (DEM) [3] to mitigate fabrication mismatch between the pull-down nMOS devices.

3.2 Analysis of Bandwidth-Resolution Tradeoffs

The proposed approach enables runtime bandwidth configuration by controlling the sampling pulse width. Measurement resolution adjusts based on the bandwidth-resolution ratio achieved by the system. Wider pulses accumulate more phase—suppressing quantization noise more effectively—while a narrower pulse allows higher bandwidth measurement.

The rectangular sampling pulse is shaped by the applied deterministic dither. Although the dither itself is applied uniformly, all time instants are not uniformly sampled across an entire dither sequence. This results in an effective pulse shape shown in Figure 3. In the figure, T_{min} is the minimum sampling pulse width, T_d is

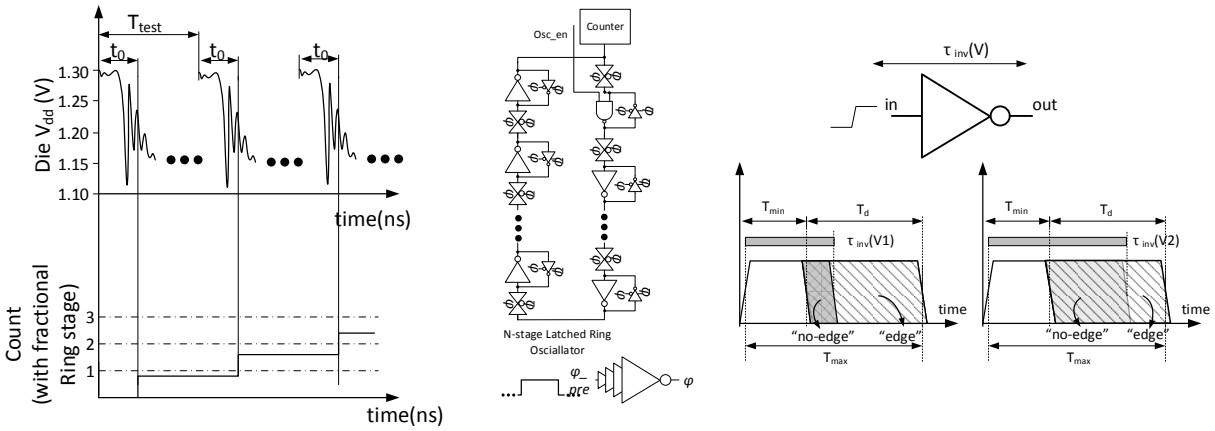


Figure 2: Proposed deterministic-dither based sampling supply noise measurement technique

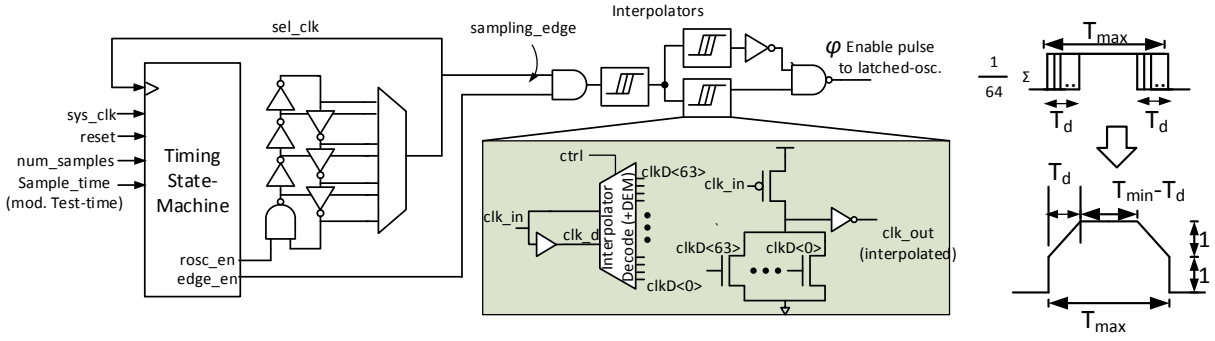


Figure 3: Proposed deterministic-dither based sampling supply noise measurement technique

the dither range, and T_{max} is the maximum sampling pulse width. Consequently, $T_{max} = T_{min} + T_d$.

The effective pulse can be viewed as a combination of three sub-waveforms, an additive square pulse and triangle pulse, and a subtractive triangle pulse. The Fourier-domain representation of the effective pulse can then be written as the sum of three Fourier representations as shown in Equation 1.

When $T_{max} \gg T_d$, the effective pulse resembles the original pulse: $f_{-3dB} = {}^{0.44}/_{Tmax}$. When $T_{min} = T_d$, the 3dB bandwidth can be shown to be $f_{-3dB} = 0.53/T_{max}$. Voltage resolution is set by the pulse width and the dither step ΔT.

Given that the measurement circuit is capable of detecting a ΔT time difference over its longest phase-accumulation duration and that T_d exceeds τ (the unit delay within the RO), voltage resolution of the proposed circuit can be shown to be:

$$\Delta V = \frac{\Delta T}{\lfloor(\frac{T_d}{\tau})\rfloor \lfloor(\frac{T_{max}}{\tau})\rfloor \frac{\partial \tau}{\partial V_{dd}}}.$$

4. SIMULATION RESULTS

In this section, we present simulation results of the proposed power supply measurement circuit. The system illustrated in Figure 3 was designed using a standard industrial 65nm CMOS process. All reported results are from post-layout extracted simulations.

From Section 3.2, the importance of ΔT in setting voltage resolution places a strong emphasis on interpolator design. Interpolator simulation results are shown in Figure 4. The maximum DNL is 0.08 of a single dither step of 650 fs resulting in 52 fs worst-case pulse jitter due to the phase interpolator.

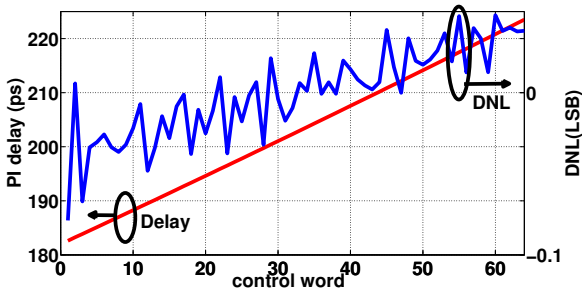
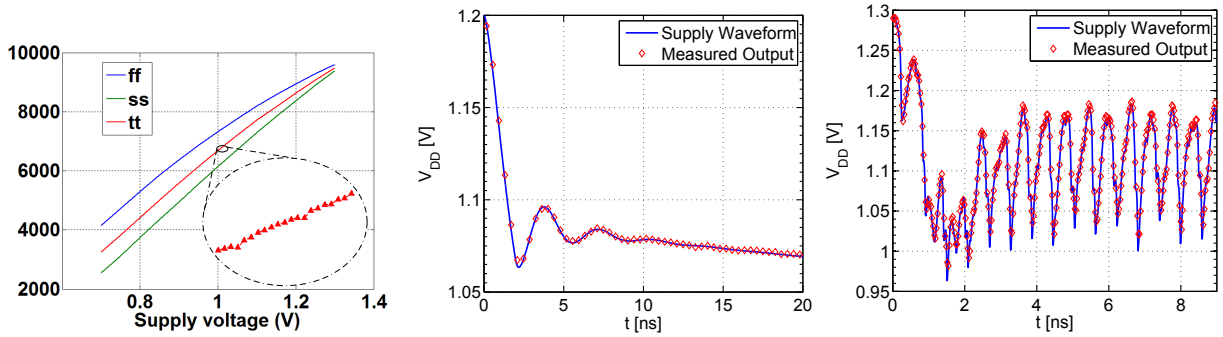


Figure 4: Phase Interpolator linearity

Figure 5a illustrates the code calibration–V_{DD} graph that is used to recover a voltage from a given code. The code displayed in the plot corresponds to 12-step dither sequence with $T_{min} = 800$ ps. Simulation was performed for fast (FF), typical (TT), and slow (SS) corners. Also shown is a finer voltage-code relationship for the TT waveform, displaying the quantization noise in the system. As expected, the simulation process corner has an impact on the V_{DD}-Code mapping. Consequently, individual calibration of each measurement system is required before post-silicon measurements.

Figures 5b and 5c illustrate the performance of the proposed supply-measurement circuit. $L^{di}/_{dt}$ supply noise caused by 1^{st} and 2^{nd} droop noise is measured with the circuit, and the reconstructed waveform is overlaid over the original supply noise waveform in Figure 5b. Measurements were taken with $T_{max} = 470$ ps, corresponding to a bandwidth of 936 MHz and an effective resolution of 0.16 mV.

$$H(f) = T_{max} sinc(T_{max} f) + \frac{T_{max}^2}{4T_d} sinc^2(\frac{1}{2} T_{max} f) - \frac{(T_{min} - T_d)^2}{4T_d} sinc^2(\frac{1}{2}(T_{min} - T_d) f). \quad (1)$$



(a) Accumulated edge count (normalized) vs. V_{DD}

(b) $L^{di}/_{dt}$ supply noise reconstruction

(c) Noise Reconstruction plots for IR supply noise

Figure 5: Simulation data. In (b), the waveform was sampled at sampled at 2.56 GHz with a nominal 430ps pulse width. In (c), the waveform was sampled at 33.3 GHz with a nominal pulse width of 40 ps.

Table 1: Performance comparison of proposed work with other supply noise measurement techniques

Performance Metric	[10]	[1] [2]	[9]	[5]	This work
Bandwidth (GHz)	6.5	44	4.1	0.7*	6.94
Samp. rate (GHz)	100	100	8.3	200	25
Voltage Res. (mV)	—**	3.2	40*,†	0.19	2.05
Area (μm^2)	1550*	—	99.79	5040*,‡	187
Test time (min.)	0.25	39960*	0.25	0.25	32
Analog I/O	Yes*	No	No	No	No
Technology (nm)	130	90	90	65	65

* Drawback † Latch-oscillator ‡ From die photo ** Analog o/p

Figure 5c illustrates an increasingly common supply noise scenario resulting from IR drop in a micro-regulated voltage domain. Since such domains are smaller in size and limited in the amount of filter decoupling capacitance they can provide, the dominant pole frequency of the impedance of the domain as seen by the load has substantially higher frequencies. In this simulation, the dominant pole frequency is 4 GHz. As seen from both figures, the proposed circuit provides very accurate reconstruction of the original IR drop dominated supply waveform.

Table 1 summarizes the performance of the proposed system along with a comparison of previously existing supply voltage monitors. In contrast to all previous works listed in the table, the proposed circuit meets all the required criterion of sufficient signal bandwidth and resolution, all-digital construction, small footprint, and reasonable test time to measure supply noise.

5. CONCLUSION

This paper presents an all digital supply noise measurement technique using a deterministic dithering technue. The proposed technique achieves bandwidth-resolution metrics beyond possible with current approaches while using a small footprint.Post-layout simulations of an implementation in an industrial 65nm process indicate an effective resolution of 2.05 mV at 6.94 GHz measurement bandwidth.

6. REFERENCES

[1] V. Abramzon et al. Scalable circuits for supply noise measurement. In *Proc. ESSCIRC 2005*, pages 463–466, Sept 2005.

[2] E. Alon, V. Abramzon, B. Nezamfar, and M. Horowitz. On-Die Power Supply Noise Measurement Techniques. *IEEE Adv. Packag.*, 32(2):248–259, May 2009.

[3] I. Galton. Why Dynamic-Element-Matching DACs Work. *IEEE Trans. Circuits Syst. II, Exp. Briefs*, 57(2):69–74, Feb 2010.

[4] A. Grenat et al. Adaptive clocking system for improved power efficiency in a 28nm x86-64 microprocessor. In *Tech. Dig. IEEE ISSCC 2014*, pages 106–107, Feb 2014.

[5] T. Hashida and M. Nagata. An On-Chip Waveform Capturer and Application to Diagnosis of Power Delivery in SoC Integration. *IEEE J. Solid-State Circuits*, 46(4):789–796, April 2011.

[6] G. Huang, M. Bakir, A. Naeemi, H. Chen, and J. Meindl. Power Delivery for 3D Chip Stacks: Physical Modeling and Design Implication. In *Proc. IEEE Elect. Performance of Electron. Packaging 2007*, pages 205–208, Oct 2007.

[7] Y. Kim et al. AUDIT: Stress Testing the Automatic Way. In *Proc. IEEE/ACM MICRO 2012*, pages 212–223, Dec 2012.

[8] N. Kurd et al. Next Generation Intel Core Micro-Architecture (Nehalem) Clocking. *IEEE J. Solid-State Circuits*, 44(4):1121–1129, Apr. 2009.

[9] Y. Ogasahara et al. All-Digital Ring-Oscillator-Based Macro for Sensing Dynamic Supply Noise Waveform. *IEEE J. Solid-State Circuits*, 44(6):1745–1755, June 2009.

[10] M. Takamiya et al. An on-chip 100 GHz-sampling rate 8-channel sampling oscilloscope with embedded sampling clock generator. In *Tech. Dig. IEEE ISSCC 2002*, volume 1, pages 182–458 vol.1, Feb 2002.

[11] Z. Toprak-Deniz et al. Distributed system of digitally controlled microregulators enabling per-core DVFS for the POWER8 microprocessor. In *Tech. Dig. IEEE ISSCC 2014*, pages 98–99, Feb 2014.