

# Fast, Efficient, Recovering, and Irreversible

Visvesh Sathe<sup>1</sup>, Juang-Ying Chueh<sup>1</sup>, Joohee Kim<sup>1</sup>, Conrad H. Ziesler<sup>3</sup>  
Suhwan Kim<sup>2</sup> and Marios C. Papaefthymiou<sup>1</sup>

<sup>1</sup> EECS Department  
U. Michigan  
Ann Arbor, MI 48109, USA

<sup>2</sup> ECE Department  
Seoul National U.  
Seoul 151-744, Korea

<sup>3</sup> MultiGig, Inc.  
Scotts Valley, CA 95066, USA

## ABSTRACT

Recent advances in CMOS VLSI design have taken us to real working chips that rely on controlled charge recovery to operate at substantially lower power dissipation levels than their conventional counterparts. In this paper, we present two such chips that were designed in our research group and highlight some of the promising charge-recovery techniques in practice. Although their origins can be traced back to the early adiabatic circuits, these techniques approach energy recycling from a more practical angle, shedding reversibility to achieve operating frequencies in excess of 1GHz with relatively low overheads.

**Categories and Subject Descriptors:** B.0 [Hardware]: General

**General Terms:** Design, Performance

**Keywords:** Charge-recovery circuits, adiabatic computing, reversible logic, resonant systems.

## 1. INTRODUCTION

Energy efficiency has become a major design concern in high-performance and mobile computer systems. Excessive power dissipation requires increasingly large, heavy, expensive, and noisy cooling machinery including special packages, heat sinks, heat pipes, and fans. Excessive energy consumption on mobile computer systems results in increasingly large, heavy, and expensive batteries, power-conversion circuits, or fuel-cells, which themselves may introduce further heat removal issues. Several effective power management design techniques have been developed over the past few years, including lowering the supply voltage. As process scaling continues below 90nm, however, it becomes more difficult to scale the supply voltage for several reasons.

To maintain high transistor drive current and thus achieve performance improvements, transistor thresholds must be scaled along with the supply voltage. However, threshold voltage scaling results in a substantial increase in subthreshold leakage current [18]. Furthermore, the uncertainty related to variations in process, voltage, and temperature is reducing the available range over which supply voltage may be scaled in an effort to reduce energy dissipation. Consequently, there is a demand for novel circuits whose power

saving mechanism is not heavily dependent on further supply voltage scaling.

Long before power consumption became a high-priority objective in computer system design, theoretical physicists had been exploring the fundamental connections of computation and power dissipation. The somewhat astonishing result of these early investigations into the energetics of computation is that the minimum energy requirements of a computation are proportional to the number of information bits destroyed during its course. Thus, if a computation could be somehow implemented without loss of information, its energy requirements could potentially be reduced to zero. Rolf Landauer and Charles Bennett at IBM were able to show, in theory, that by performing computations in a *reversible* manner, no information is destroyed and thus potentially zero energy would be needed [4]. Further work demonstrated concrete transformations that can map ordinary computations into reversible computations.

The idea of a reversible computation is pretty straightforward. A system is reversible if no information about its state is lost at any time during its transformation. For example, if  $2 + 2$  is computed, a reversible computing system would pass on 4 as the answer, exactly as a standard one would. Furthermore, a reversible system would also save at least one of the operands, so it could reverse the computation. If it didn't, then it would not necessarily know if the two operands were 1 and 3, 2 and 2, or 0 and 4, resulting in loss of information and unrecoverable energy costs.

While reversibility is required for zero energy consumption, it is by no means sufficient. Since the mere transfer of a charge across a voltage difference is the result of energy exchange, some circuit embodiment is still needed in addition to reversibility to actually compute with zero dissipation. The set of circuit design techniques targeted at the implementation of computations with minimal (asymptotically zero) power consumption during charge transfer is generally known as *adiabatic switching* or *adiabatic charging*.

Ideally, by increasing the time  $T_s$  over which computation is performed and by using reversible logic to avoid the destruction of information, it should be possible to create a circuit which computes with vanishingly low energy dissipation as the time allowed for that computation extends indefinitely. Known in the field as "asymptotically zero energy consumption," this possibility might have remained a mere theoretical curiosity had not a dedicated community of researchers worked on creating first theoretical and later practical circuit implementations of logic and state elements. These circuit implementations applied some of the principles of reversible computing and adiabatic charging to achieve low, but nonzero, dissipation for computations performed over fixed amounts of time. Over time, the strict requirements of reversibility were dropped, giving way to engineering compromises that have led to practical

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

CF'05, May 4–6, 2005, Ischia, Italy.

Copyright 2005 ACM 1-59593-019-1/05/0005...\$5.00.

systems. Because some of the energy in these circuits (in the form of charge stored on capacitances) was being recovered instead of dissipated, the terms *charge recovery* or *energy recycling* began to be used to describe these circuits. Broadly speaking, the term charge recovery is nowadays being used to describe systems that reclaim some of the energy that is stored in their capacitors during a computation and reuse it on subsequent computations. These systems are not necessarily reversible.

This paper focuses on two irreversible yet charge-recovery chips that have been developed in the Advanced Computer Architecture Laboratory at the University of Michigan. The first chip is a 130MHz dynamic multiplier designed in a source-coupled adiabatic dynamic logic [9, 10] and fabricated in  $0.5\mu\text{m}$  bulk silicon. The second chip is a 300MHz resonant-clocked ASIC for the Discrete Wavelet Transform that has been synthesized using industry-standard tools [25] and has been fabricated in a  $0.25\mu\text{m}$  bulk silicon process. A third design which is discussed in the paper, is an energy recovery logic family which has been successfully simulated at operating frequencies greater than 1.6GHz in post-layout simulations.

None of the designs in this paper performs reversible computations. All designs rely on on-chip circuitry to generate a single-phase or a two-phase power-clock waveform of sinusoidal shape. With measured power savings at clock rates in the 100–300MHz range, our chips provide tangible evidence that charge recovery approaches can yield highly energy-efficient designs in practice. They also provide experimental evidence revealing another important and largely unexplored advantage of charge-recovery circuitry, namely their low electromagnetic interference.

The remainder of this paper has four sections. Section 2 describes the multiplier chip. Section 3 describes the resonant-clocked ASIC chip. Section 4 highlights our GHz-class logic-family. Section 5 summarizes the paper and concludes with directions for further research.

## 2. DYNAMIC MULTIPLIER

This section describes a full-custom multiplier chip we implemented in a dynamic source-coupled charge-recovery logic family. The chip relies on a true single-phase power-clock waveform to provide power and synchronization. Single-phase energy recovery enjoys several distinct advantages over multiphase approaches. First, single-phase clocking imposes less stringent requirements on clock distribution than multiple-phase clock schemes. Most notably, the need to control the relative skew of multiple clock phases is completely eliminated. Second, power-clock generation is more efficient with a single phase than with multiple phases. Specifically, data dependencies may cause significant variations in power-clock currents and can be detrimental to the efficiency of the power-clock generator. In single-phase systems, tolerating such variations through feedback control in the power-clock generator presents fewer challenges than in multiphase systems.

The chip does not perform any reversible computation in its logic blocks. It does rely on some notion of “balanced operation”, however, to allow for the efficient recycling of charge. In particular, the multiplier uses dual-rail gates, with charge recovery taking place all the way to the gate fanouts. At each gate, the loading of the two fanout nets is essentially the same. Thus, at each cycle of the computation the same amount of charge is stored on one or the other rail, depending on the output of the function, and the overall load of the power-clock generator remains relatively stable.

The 8-bit charge-recovery multiplier was designed using the source-coupled adiabatic logic family SCAL-D [8] and a  $0.5\mu\text{m}$  single-poly triple-metal  $n$ -well CMOS process supplied through MOSIS. In HSPICE simulations with parasitics extracted from layout, the

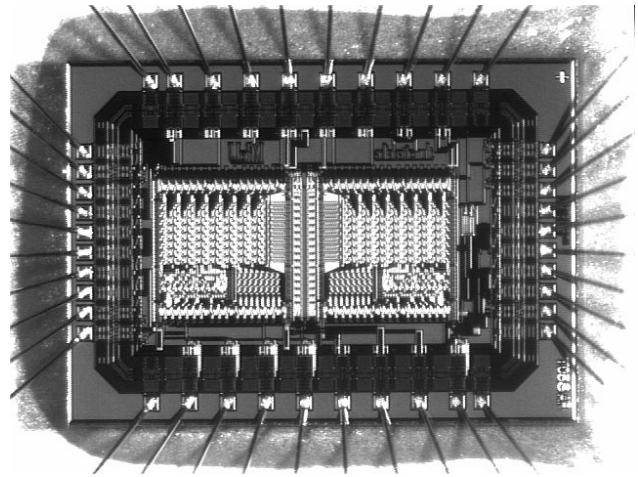


Figure 1: Microphotograph of the true single-phase multiplier chip.

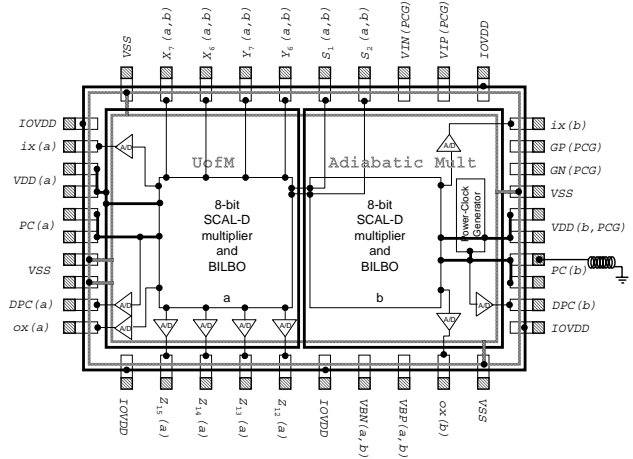


Figure 2: Simplified floorplan of the chip in Figure 1.

multiplier achieved operating speeds up to 200MHz, and test results (limited by our experimental setup) confirmed its correct operation for clock rates up to 140MHz. Our chip was first presented in [9], while a more detailed description and comparative evaluation followed in [10]. In this section, we summarize and highlight key aspects of the design.

A die photo and simplified floorplan of our chip are shown in Figures 1 and 2, respectively. Each die includes two 8-bit charge-recovery multipliers with charge-recovery built-in logic block observer (BILBO) circuitry, a power-clock generator, adiabatic-to-digital converters (denoted by A/D), and conventional I/O pads. Total chip area is  $4.83\text{mm}^2$  ( $= 2.60\text{mm} \times 1.84\text{mm}$ ).

Figure 3 shows a typical pipeline of gates from the logic family SCAL-D that was used in the multiplier chip. This particular pipeline implements a 2-bit shift-register. Each pipeline stage consists of one PMOS and one NMOS SCAL-D gate, each computing on the rising and falling edges of the single-phase power-clock signal, respectively. Notice that this circuit is micropipelined, with fine-grain charge recovery taking place all the way from the fanouts of the individual gates. The level-shifter blocks LSP and LSN provide appropriate biases for the correct operation of the PMOS and

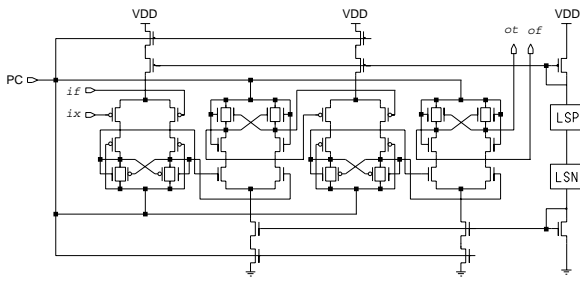


Figure 3: Shift-register in adiabatic logic family SCAL-D.

NMOS gates.

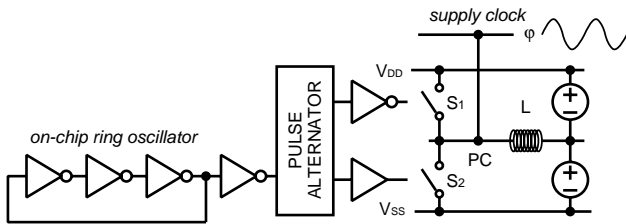


Figure 4: Power-clock generator for multiplier chip.

Figure 4 shows the power-clock generator circuit that was used with the multiplier chip. Except for the inductor, all clock generator circuitry was integrated on the chip. The power-clock generator relies on Class-E amplifier principles to achieve high energy efficiency. Specifically, the switches  $S_1$  and  $S_2$  replenish the energy of the power-clock waveform every cycle, conducting current when the voltage difference across their terminals is minimal. The timing of the two switches is controlled by a pulse alternator circuit that receives a pulse train from the ring oscillator at a rate equal to the target operating frequency and generates two pulse trains of the same rate and 180 degrees out of phase.

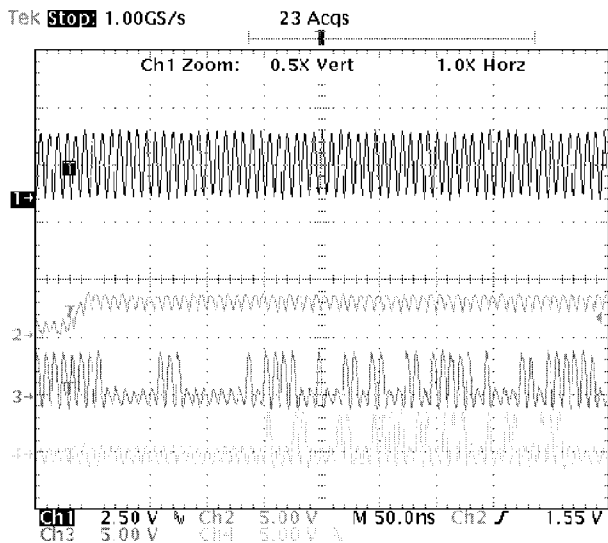


Figure 5: Measured waveforms of 8-bit SCAL-D multiplier with associated BIST logic in self-test mode at 130MHz.

Figure 5 demonstrates the correct operation of the SCAL-D chip at an operating frequency of 130MHz. This figure shows the power-

clock (channel 1), a BILBO control signal (channel 2), and the output sequences of BILBO-1 and BILBO-2 (channels 3 and 4).

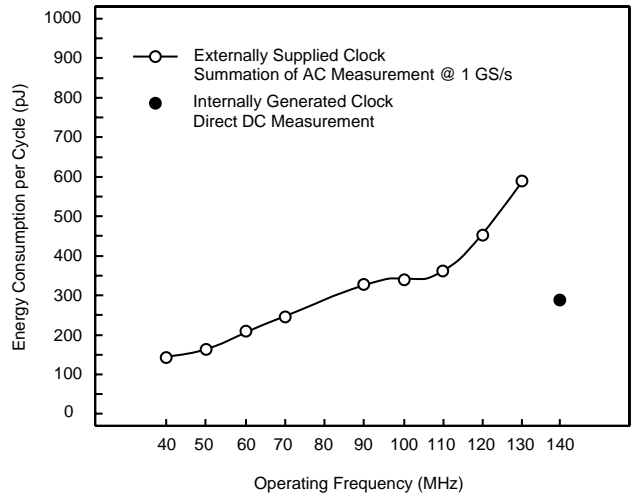


Figure 6: Measured energy consumption per cycle for various PMOS/NMOS biasing voltages.

Figure 6 gives the energy consumption of the 8-bit SCAL-D multiplier and associated BIST logic for various PMOS and NMOS biasing voltages. Measurements in the 40–130MHz frequency range were obtained using an external source of power-clock, with both the amplitude of the sinusoidal power-clock  $V_{PC}$  and the constant supply voltage  $V_{dd}$  set to 3.0V. At 140MHz, the measurement was obtained for the combined clock generator and multiplier system also at 3.0V.

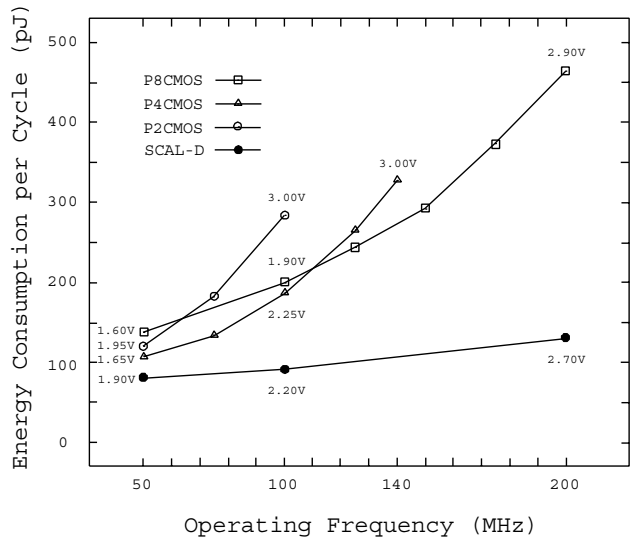
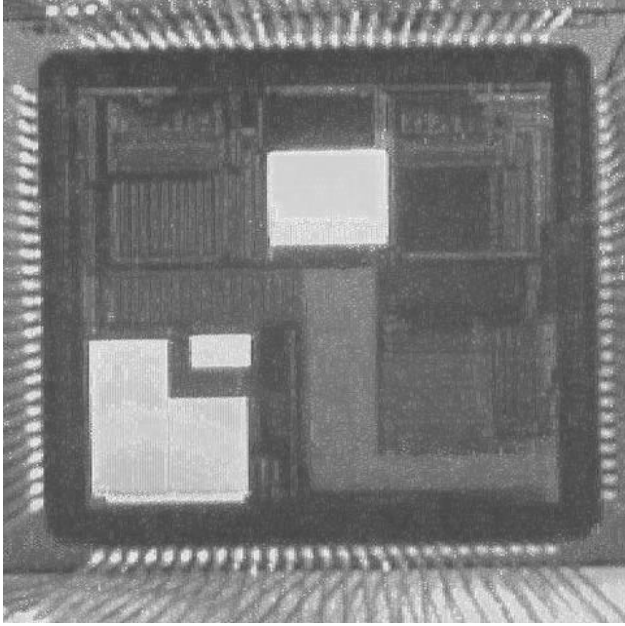


Figure 7: Energy consumption per cycle for charge recovery multiplier and conventional pipelined counterparts in static CMOS.

To evaluate the relative efficiency of our charge recovery multiplier, we synthesized and simulated conventional static CMOS multipliers with 2, 4, and 8 pipeline stages. At equal throughputs, our HSPICE simulations of voltage-scaled designs predicted energy savings up to a factor of 4, as shown in Figure 7. In all cases, the latency of our charge recovery multiplier was 15 cycles.

### 3. RESONANT-CLOCKED ASIC



**Figure 8: Microphotograph of the resonant clocked ASIC chip.**

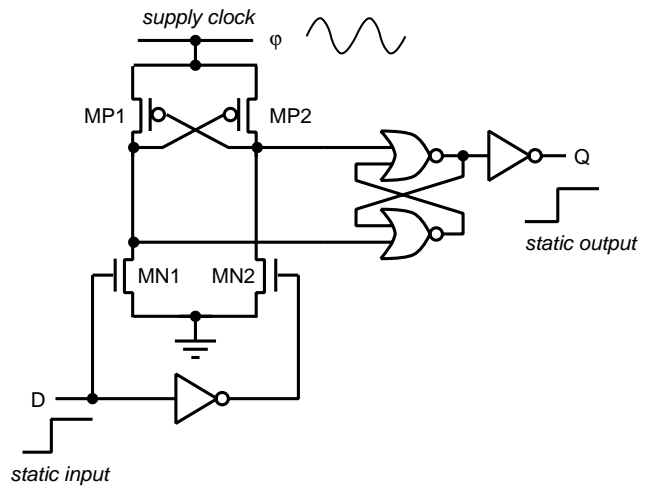
We recently designed and tested a synthesized ASIC that performs a 7-bit Discrete Wavelet Transform. The chip was fabricated in a  $0.25\mu\text{m}$  bulk-CMOS process through MOSIS. Comprising close to 4,000 gates, our ASIC is clocked by a resonant charge-recovering waveform of sinusoidal shape. Figure 8 shows a microphotograph of our resonant-clocked chip [25]. The lower left corner of the die contains our experimental energy-recovering design that consists of an ASIC core, an on-chip resonant clock generator, and some testing logic. The energy recovering flip-flops are driven by a resonant clock waveform generated using an off-chip surface-mount inductor and an on-chip power-clock generator.

Just like the multiplier, our ASIC chip does not perform any reversible computation in its logic blocks. In some sense, however, this it does perform charge recovery in a “reversible” aspect of its operation, since the state of the clock toggles between 0 and 1 every clock cycle.

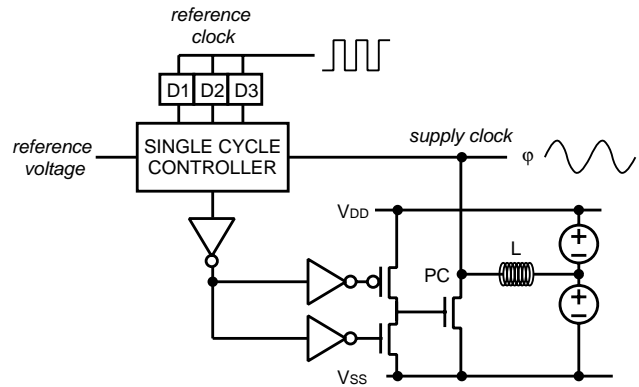
A schematic of the energy-recovering flip-flop used in our ASIC is shown in Figure 9. This flip-flop consists of a charge recovering dynamic buffer driving a pair of cross-coupled NOR gates as the static latch element. Our flip-flop latches on rising pulses of power-clock. The input needs to be stable by the time power-clock is roughly half way to its peak, and should be held stable until power-clock is at the peak. The flip-flop draws more current from the power-clock when active (i.e., the data is changing), thus changing the effective load seen by the power-clock generator.

Our chip includes a single-cycle feedback control resonant power-clock generator, shown in Figure 10, that is capable of reacting to changes in its load. The amplitude of the power-clock signal is sampled and compared against a reference level. The result of this comparison is used to decide, on a cycle-by-cycle basis, whether or not to turn on the main NMOS power-switch to pump more energy into the power-clock. This control is critical for achieving ultra-low dissipation when the ASIC is idling.

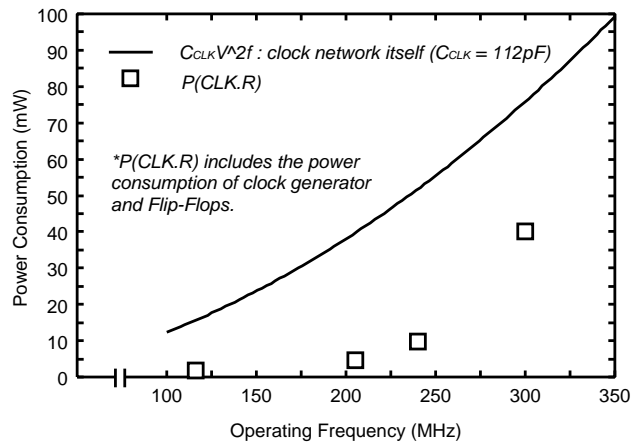
Figure 11 shows the measured energy dissipation of the clock network in our resonant-clocked ASIC chip at several frequencies between 100MHz and 300MHz. At each frequency point, the volt-



**Figure 9: Energy recovering sinusoidal flip-flop used in the resonant clocked ASIC chip.**



**Figure 10: Clock generator used in ASIC chip.**



**Figure 11: Measured power consumption resonant-clocked ASIC.**

age was scaled down to the minimum required for correct operation. The inductor and DC supplies were connected externally. For reference, we plot a quadratic curve fit to the function  $fCV_{dd}^2$  evaluated at each of the voltage, frequency pairs. This curve rep-

represents the dissipation required to drive the same clock capacitance if charge recovery techniques were not used. At  $f=300\text{MHz}$ , the clock was overdriven using an inductance value larger than  $1/C(2\pi f)^2$ , resulting in suboptimal power dissipation at that frequency. At  $205\text{MHz}$ , the measured clock power dissipation was  $4.5\text{mW}$ , about 5 times less than required to drive the same clock capacitance with conventional means. These dramatic power savings are due to operation near the resonance of the inductor in conjunction with the clock-capacitance.

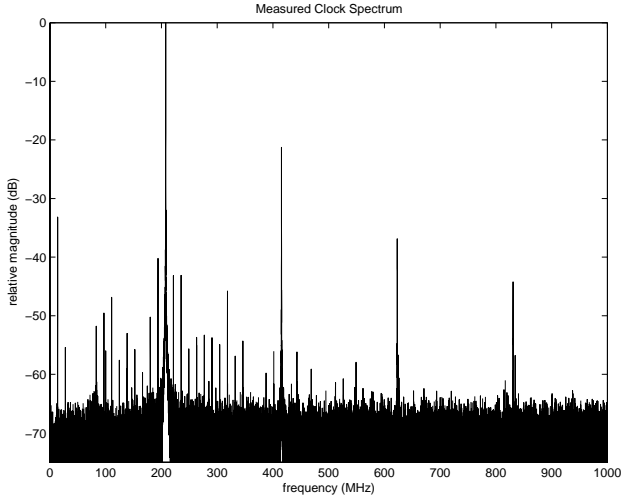


Figure 12: Measured power-clock spectrum, 200MHz.

In addition to reduced power dissipation, charge recovery circuitry has the potential to operate with substantially reduced electromagnetic interference. To provide empirical evidence in support of this largely unexplored fact, we analyzed the spectrum of the measured power-clock waveform when resonating at  $200\text{MHz}$ . The spectrum obtained is shown in Figure 12, zoomed in on the region of interest from 0 to  $1\text{GHz}$ . This data was obtained by recording  $100,000$  voltage samples at  $100\text{ps/sample}$  at the off-chip inductor terminal. Assuming linear characteristics from the parasitic elements between the inductor terminal and the on-chip clock network, this data should be proportional to the actual clock signal on-chip. The graph shows the presence of substantially attenuated odd and even harmonics. Specifically, the first 3 harmonics are  $22\text{dB}$ ,  $36\text{dB}$ , and  $43\text{dB}$  below the fundamental, respectively. In contrast, the first harmonic of a square waveform at  $600\text{MHz}$  is about  $12\text{dB}$  below the fundamental. The spur at roughly  $10\text{MHz}$  can be attributed to a periodicity in the datapath self-test activity as it corresponds roughly to the spectrum of one of the self-test signature outputs. An alternate hypothesis is that it results from some coupling with one of the I/O pads slewing.

#### 4. GHZ-CLASS LOGIC

We have recently developed a fine-grained hybrid logic that consists of conventional switching and charge-recovery stages called Boost Logic [19]. The proposed hybrid logic achieves substantially higher energy efficiency than its conventional counterparts, trading off increased higher power efficiency for increased latency at frequencies of over  $1.5\text{GHz}$ . To assess the energy efficiency and performance of our proposed logic family, we designed an 8-bit multiplier entirely in Boost Logic. In post-layout simulations of our multiplier that include interconnect and device parasitics (including the on-chip inductor), the circuit dissipates  $6.9\text{pJ/cycle}$  in the logic

and the two-phase clock generator at  $1.6\text{GHz}$ . Moreover, correct operation is achieved even if the two phases are off by up to 15% of the clock period. In comparison with a synthesized voltage-scaled multiplier that was designed in conventional CMOS with sufficient pipelining to achieve the same throughput, our charge-recovery design achieves energy savings in excess of 65% at  $1.6\text{GHz}$ . In the following section, we will discuss the structure and operation of Boost Logic and consider its robustness to clock skew in the context of resonant clocks.

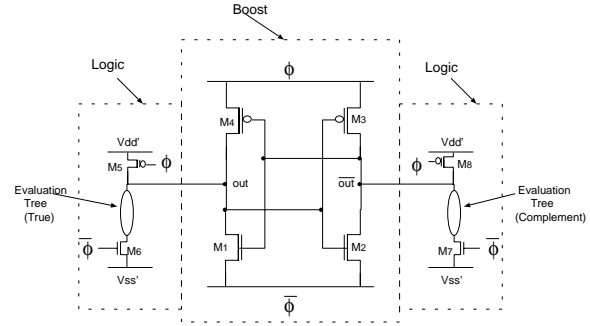


Figure 13: Boost Logic

Figure 13 shows a typical Boost Logic logic gate. Boost Logic is a two-phase, dual-rail, partially energy recovering n-n logic. The operation of a Boost gate can be divided into two parts—logical evaluation (“Logic”) and boost conversion (“Boost”). The logic stage comprises a dual-rail pseudo nMOS evaluation tree. The design of the logic stage differs from conventional pseudo nMOS evaluation in that the weak pMOS pull-up and the footer transistor both turn on only during the evaluation of the logic stage. At other times, they are off, isolating the output node from the conventional voltage supply rails. The pseudo nMOS-like gate is chosen to reduce the loading on the gate thereby improving performance. For the purpose of robustness, the weak pMOS pullup can be made strong and a complementary pullup pMOS evaluation tree be added in series. The power supply rails are at voltages:

$$V_{dd}' = \frac{1}{2} \cdot (V_{dd} + V_{th}), \quad (1)$$

$$V_{ss}' = \frac{1}{2} \cdot (V_{dd} - V_{th}). \quad (2)$$

This choice of voltage values is motivated by the operation of the boost stage. The potential difference between the voltage supply rails in the logic stage is therefore  $V_c = V_{th}$ . The boost stage, which is essentially an energy recovering sense amplifier, resembles back-to-back CMOS inverters. The only difference is that the  $V_{dd}$  and  $Gnd$  rails are replaced by  $\phi$  and  $\bar{\phi}$ .

Boost Logic utilizes a dual-rail gate structure to ensure that the capacitance presented to the power-clock by the gate is balanced and data-independent, reducing clock jitter. The use of the pseudo nMOS-type evaluation tree reduces the input loading of the gate at the expense of short-circuit dissipation in the gate. The delay penalty due to the header and footer can be reduced by sizing up transistors  $M5$ ,  $M6$ ,  $M7$ , and  $M8$ . Since the gate inputs to these transistors are resonant clocks, wider transistors result in significantly lower energy penalties compared to a conventional clock. To reduce the susceptibility of gate performance to process variation, a complementary pMOS evaluation tree can be used in series with  $M5$  and  $M8$ .

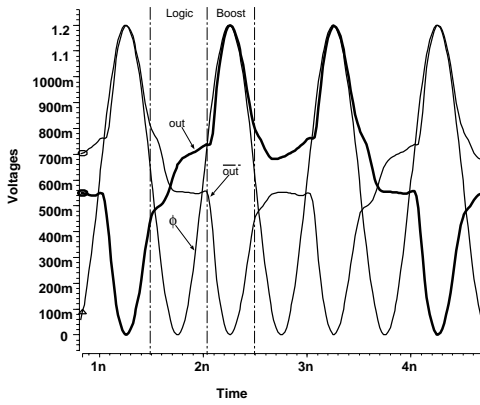


Figure 14: SPICE waveforms of a Boost Logic inverter

Figure 14 illustrates the operation of a Boost inverter. The complementary clock waveform  $\bar{\phi}$  is not shown in the figure but is exactly in anti-phase with  $\phi$ . By design, the logic and boost stages evaluate at mutually exclusive intervals. As such, when the logic stage evaluates, the boost stage does not drive the outputs and vice-versa. Consider the operation of the gate whose waveforms are shown in Figure 14. When the logic stage evaluates ( $\phi$  falls and  $\bar{\phi}$  rises), the header transistors  $M_5$  and  $M_8$  and footer transistors  $M_6$  and  $M_7$  turn on. As  $out$  evaluates high, the header transistor  $M_5$  pulls the output node to  $V_{dd}'$ . The complementary output discharges through the evaluation tree to nearly  $V_{ss}'$ . At this time, the energy recovering sense amplifier is in pre-charge with  $\phi = 0$  and  $\bar{\phi} = V_{dd}$ . In this state, it is easily verified that as long as the outputs stay within the conventional supply rails, none of the transistors in the sense amplifier are turned on, and no crowbar current flows in the Boost converter. As  $\phi$  begins to rise past  $V_{ss}'$  (or 450mV in Figure 14), the logic stage is deactivated, disconnecting  $out$  and  $\bar{out}$  from  $V_{dd}'$  and  $V_{ss}'$ . As  $\phi$  continues to rise past  $V_{dd}'$ , the boost conversion begins to operate. Since  $out$  is at  $V_{dd}'$  and  $\bar{out}$  at nearly  $V_{ss}'$ , transistors  $M_2$  and  $M_4$  turn on as  $\bar{\phi}$  ( $\phi$ ) goes past  $V_{ss}'$  ( $V_{dd}'$ ), causing  $\bar{out}$  ( $out$ ) to subsequently follow  $\bar{\phi}$  ( $\phi$ ). During boost conversion, as the voltage difference between  $out$  and  $\bar{out}$  increases, transistors  $M_2$  and  $M_4$  turn more strongly on, reducing the voltage difference across the current-carrying transistors further. Finally, the nodes  $out$  and  $\bar{out}$  reach the rails  $\phi$  and  $\bar{\phi}$ , respectively. These outputs will drive the next gate during its logical evaluation stage.

As  $\phi$  and  $\bar{\phi}$  transition once again, entering the next logic phase, the outputs track the corresponding complementary clocks once again through the same transistors  $M_2$  and  $M_4$ . As the voltage difference between  $out$  and  $\bar{out}$  approaches  $V_{th}$ , conduction in any of the four transistors in the sense amplifier stops and the logic stage once again begins to evaluate.

Boost Logic achieves energy recovery at high frequencies due to several design features. First, the boost converter stage in Boost Logic does not require diodes to perform energy recovery and can therefore operate efficiently at relatively higher frequencies. Being an n-n logic, Boost Logic eliminates the use of pMOS evaluation trees, greatly reducing capacitive loading of gate inputs in spite of being a dual-rail logic and enhancing speed. Also, Boost gates pre-charge to nearly  $1/2V_{dd}$  which reduces the output swing of the gate and therefore the energy dissipated in the boost stage. By not having to follow the power-clock when it transitions at its fastest rate ( $1/2V_{dd}$  for sinusoidal clocks), higher operating frequencies are possible for a given energy efficiency. This form of pre-charge also provides more time for the logic stage of the gate to evaluate

as compared to energy recovery designs that pre-charge to nearly  $V_{dd}$  or  $Gnd$ .

Another feature of Boost Logic that enables its high frequency operation is the fact that the pseudo nMOS structure in the logic stage produces complementary output nodes with a voltage difference of nearly  $V_c$ . Thus, the gate outputs are not left unresolved at the onset of boost conversion, precluding any “fight” between the output nodes of the energy recovering sense amplifier and resulting in efficient boost conversion. The absence of any conflict in the sense amplifier during the operation of the Boost stage also provides a data-independent capacitance to the clock generator, minimizing data induced jitter.

Boost Logic has proven to be substantially robust to clock skew. From post-layout simulations, Boost Logic was characterized to operate correctly with skew amounting to 15% of the clock cycle. We have also performed post-layout simulations of a resonant clock tree spanning a 2mm-square area, focusing on the effect of clock skew and jitter due to static and dynamic load imbalance. Our simulations indicate a worst-case skew of 8.5% of the clock period at frequencies above 790MHz [5]. The skew tolerance of Boost Logic was therefore found to be sufficient for correct operation.

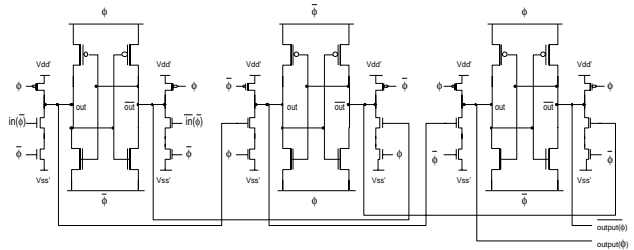


Figure 15: Cascade of Boost Logic inverters

Cascading Boost gates is straightforward. The connection for a chain of inverters is shown in Figure 15. Observe that from a timing (and to a large extent, functional) perspective, a boost gate consists of a conventional gate driving a level-converting latch. As in latch-based design, Boost Logic is cascaded with alternating  $\phi$  and  $\bar{\phi}$  gates.

## 5. CONCLUSION

The field of charge recovery has come a long way from its origins in the physics of computation. Originally merely a theoretical curiosity, it is approaching maturity as several researchers independently producing functional prototypes in conventional silicon CMOS fabrication processes. In contrast to other low-power design techniques, which try to reduce power by performing less wasted computation, parallelizing the computation, or lowering supply voltage, charge recovery fundamentally changes the shape of the dissipation vs. delay and area trade-offs, allowing for sub- $fCV_{dd}^2$  dissipation with the help of novel circuits implemented in standard CMOS processes.

This paper has focused on two charge-recovery chips and a gigahertz-class logic family designed in our research group at the University of Michigan. There is a rich context of prior work, however, such as the reversible and irreversible designs described in [2, 3, 6, 11, 12, 13, 14, 15, 17, 22, 24]. Moreover, charge-recovery design technologies have shown great promise in reducing the power consumption of other key components in digital computing systems such as, for example, high-speed rotary clocks in [23], low-power memory arrays including SRAMs and register files [7, 16, 20, 21], and low-power drivers for LCD displays [1]. The future

of charge recovery appears more promising than ever. With the advent of design automation tools and the increasing familiarization of designers with charge recovery design technologies, we can expect commercial chips in certain power- or energy-sensitive areas to adopt some form of energy recycling in the near future.

## 6. ACKNOWLEDGMENTS

This research was supported in part by the US Army Research Office under Grant Nos. DAADA19-03-1-0122 and DAAD 19-99-1-0304 and by the Defense Advanced Research Projects Agency under Contract No. N66001-02-C-8059.

## 7. REFERENCES

- [1] M. Amer, M. Bolotski, P. Alvelda, and T. Knight. A 160x120 pixel liquid-crystal-on-silicon microdisplay with an adiabatic dac. In *IEEE International Solid-State Circuits Conference*, November 1999.
- [2] W. Athas, N. Tzartzanis, W. Mao, L. Peterson, R. Lal, K. Chong, J.-S. Moon, L. Svensson, and M. Bolotski. The design and implementation of a low-power clock-powered microprocessor. *IEEE Journal of Solid-State Circuits*, SC-35(11):1561–1570, November 2000.
- [3] W. C. Athas, N. Tzartzanis, L. J. Svensson, and L. Peterson. A low-power microprocessor based on resonant energy. *IEEE Journal of Solid-State Circuits*, SC-32(11):1693–1701, November 1997.
- [4] C. H. Bennett and R. Landauer. The fundamental physical limits of computation. *Scientific American*, 253(1):38–46, July 1985.
- [5] J. Chueh, C. Ziesler, and M. Papaefthymiou. Two-phase resonant clock distribution. In *Unpublished Manuscript*, 2005.
- [6] M. Frank. Reversibility for efficient computing. *Ph.D. thesis, MIT*, 1999.
- [7] J. Kim, C. H. Ziesler, and M. C. Papaefthymiou. Energy recovering static memory. In *Proceedings of International Symposium on Low-Power Electronics and Design*, August 2002.
- [8] S. Kim and M. C. Papaefthymiou. Single-phase source-coupled adiabatic logic. In *Proceedings of International Symposium on Low-Power Electronics and Design*, pages 97–99, August 1999.
- [9] S. Kim, C. Ziesler, and M. C. Papaefthymiou. A true single-phase 8-bit adiabatic multiplier. In *Proc. 38th ACM/IEEE Design Automation Conference*, June 2001.
- [10] S. Kim, C. H. Ziesler, and M. C. Papaefthymiou. A true single-phase energy-recovery multiplier. *IEEE Transactions on VLSI Systems*, (2):194–207, April 2003.
- [11] A. Kramer, J. S. Denker, S. C. Avery, A. G. Dickinson, and T. R. Wik. Adiabatic computing with the 2N-2N2D logic family. In *Digest of Technical Papers of IEEE Symposium on VLSI Circuits*, pages 25–26, April 1994.
- [12] A. Kramer, J. S. Denker, B. Flower, and J. Moroney. 2nd order adiabatic computation with 2N-2P and 2N-2N2P logic circuits. In *1995 International Symposium on Low Power Design*, pages 191–196, 1995.
- [13] J. Lim, D. Kim, and S. Chae. A 16-bit carry-lookahead adder using reversible energy recovery logic for ultra-low-energy systems. *IEEE Journal of Solid-State Circuits*, SC-34(6):898–903, June 1999.
- [14] D. Maksimovic, V. G. Oklobdzija, B. Nikolic, and K. W. Current. Clocked CMOS adiabatic logic with integrated single-phase power-clock supply. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 8(4):460–463, August 2000.
- [15] Y. Moon and D. Jeong. An efficient charge recovery logic circuit. *IEEE Journal of Solid-State Circuits*, SC-31(4):514–522, April 1996.
- [16] Y. Moon and D. K. Jeong. A 32x32-b adiabatic register file with supply clock generator. *IEEE Journal of Solid-State Circuits*, SC-33(5):696–701, May 1998.
- [17] V. G. Oklobdzija and D. Maksimovic. Pass-transistor adiabatic logic using single power-clock supply. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, 44(10):842–846, October 1997.
- [18] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand. Leakage current mechanism and leakage reduction techniques in deep-submicrometer CMOS circuits. *Proceedings of the IEEE*, 91(2):305–327, February 2003.
- [19] V. Sathe, C. Ziesler, and M. Papaefthymiou. Boost logic: A high speed energy recovery circuit family. In *Unpublished Manuscript*, 2005.
- [20] D. Somasekhar, Y. Ye, and K. Roy. An energy recovering static RAM memory core. In *Proceedings of International Symposium on Low Power Design*, April 1995.
- [21] N. Tzartzanis, W.C. Athas, and L. Svensson. A low-power SRAM with resonantly powered data, address, word, and bit lines. In *European Solid-State Circuits Conference*, 2000.
- [22] C. Vieri. Reversible computer engineering and architecture. *Ph.D. thesis, MIT*, 1999.
- [23] J. Wood, T. Edwards, and S. Lipa. Rotary travelling-wave oscillator arrays: a new clock technology. *IEEE Journal of Solid-State Circuits*, SC-36(11):1654–1665, November 2001.
- [24] S. G. Younis. Asymptotically zero energy computing using split-level charge recovery logic. *Ph.D. thesis, MIT*, 1994.
- [25] C. Ziesler, J. Kim, V. Sathe, and M. C. Papaefthymiou. A 225MHz resonant clocked ASIC chip. In *Proc. of International Symposium on Low-Power Electronics and Design*, August 2003.